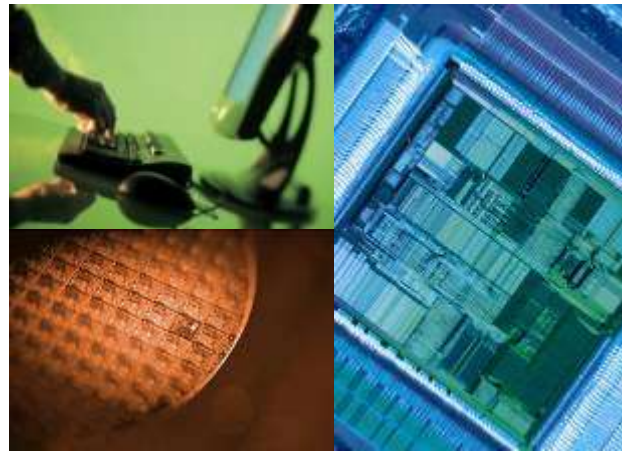


Low Power Trends and Methodology

Godwin Maben





Agenda

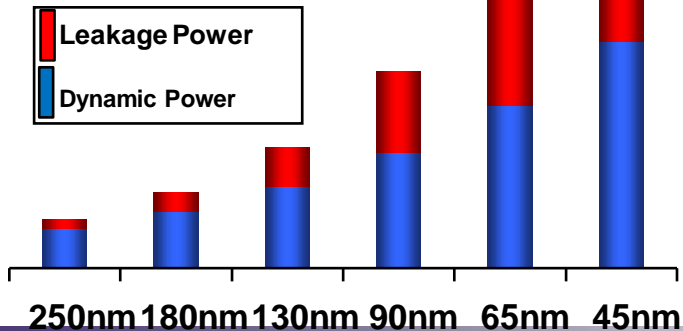
- Introduction
- Summary of Low Power Techniques
 - Designer's Arsenal
- Details on each Technique
 - Technology Highlights
 - Advantages/Trade-Offs
 - Challenges
- Synopsys Low Power Flow Summary

Reasons for Low Power Demand

Power Consumption of the World's Processors through 2006

Year	Power (in megawatts)	# CPUs (in millions)
1992	160	87
1993	250	106
1994	392	128
1995	613	156
1996	959	189
1997	1,501	230
1998	2,349	279
1999	3,676	339
2000	5,752	412
2001	9,000	500
2002	14,083	607
2003	22,038	737
2004	34,485	896
2005	53,962	1,088
2006	84,439	1,321

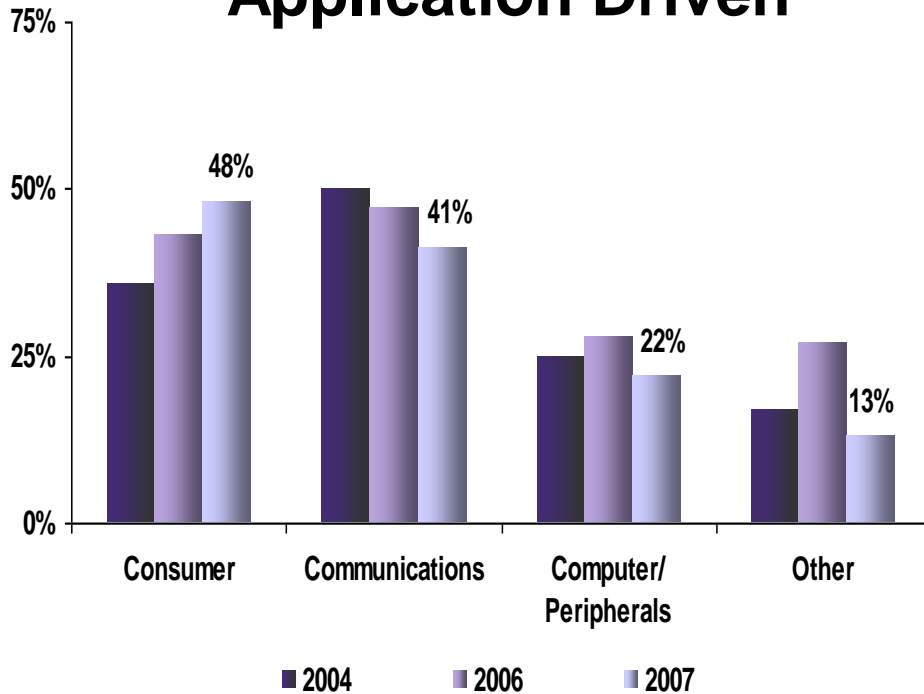
Source: Intel



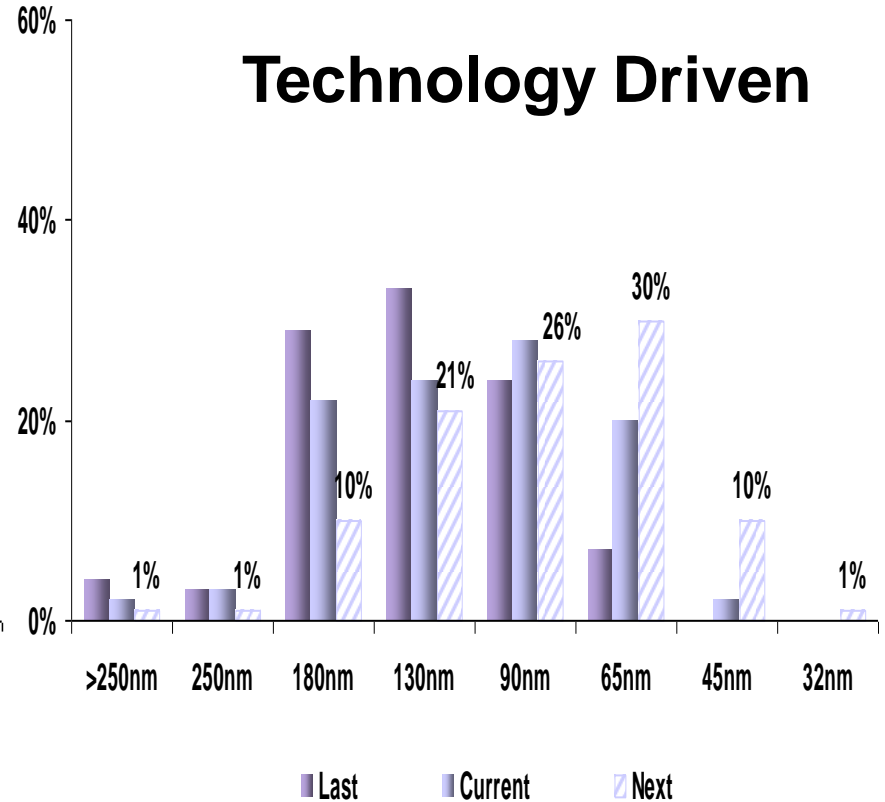
It's all about battery life

Reasons for Low Power Demand

Application Driven



Technology Driven



Source: SNUG 2007

Summary of Low Power Techniques (Designer's Arsenal)

Factors Governing Power

$$E = \int_0^t (V_{DD}I_{leak} + CV_{DD}^2 f_c) dt$$

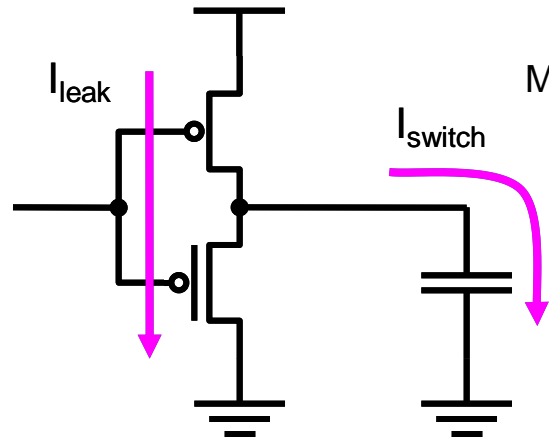
Total Power Dissipation

$$\int_0^t V_{DD}I_{leak} dt$$

Static Power Dissipation

Dynamic Power Dissipation

$$\int_0^t CV_{DD}^2 f_c dt$$



Minimize I_{leak} by:

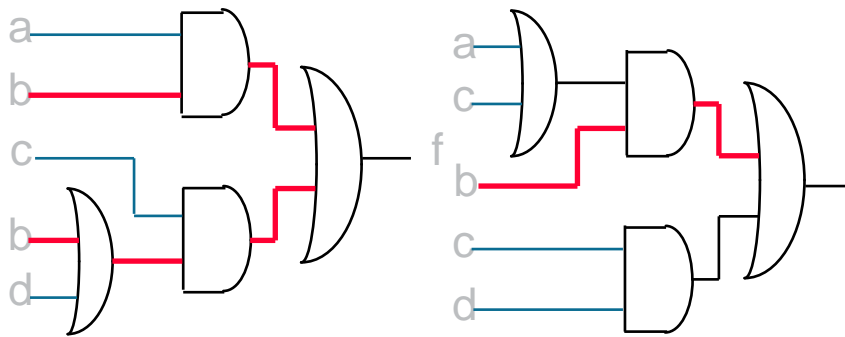
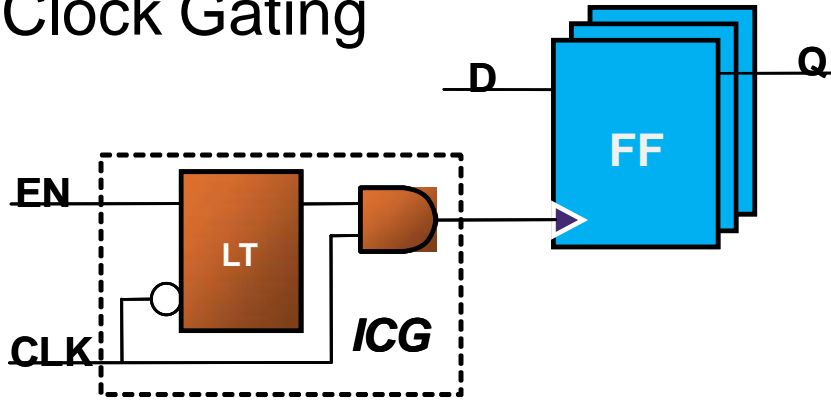
- Reducing operating voltage
- Fewer leaking transistors

Minimize I_{switch} by:

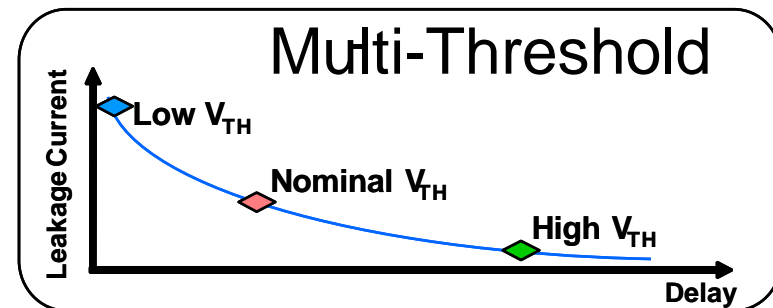
- Reducing operating voltage
- Less switching cap
- Less switching activity

Basic Low Power Techniques Summary

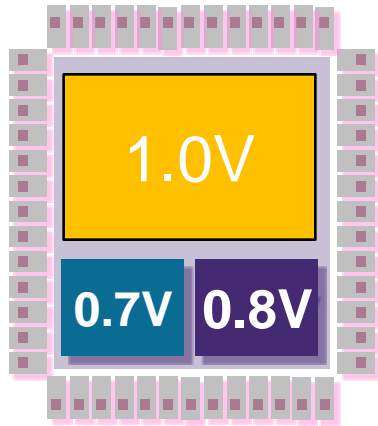
Clock Gating



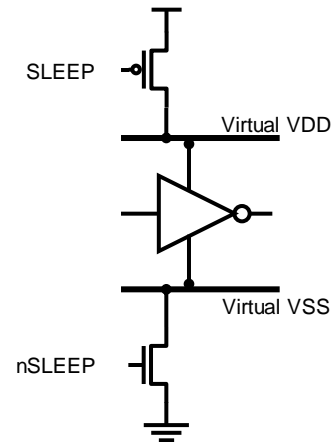
	16 bit	64 bit
Ripple	90	366
CLA	100	405
Carry Skip	108	437
Carry Select	161	711
Carry Save	218	1323



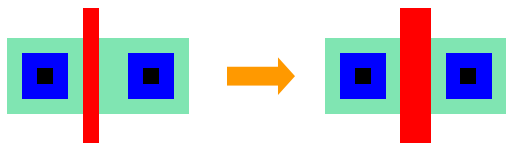
Advanced Low Power Techniques Summary



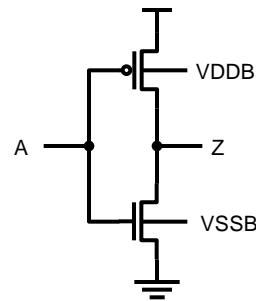
Multi-Voltage (MV)



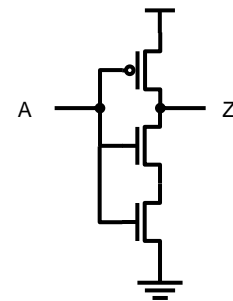
Power Gating



Non minimum size gate lengths



VTCMOS

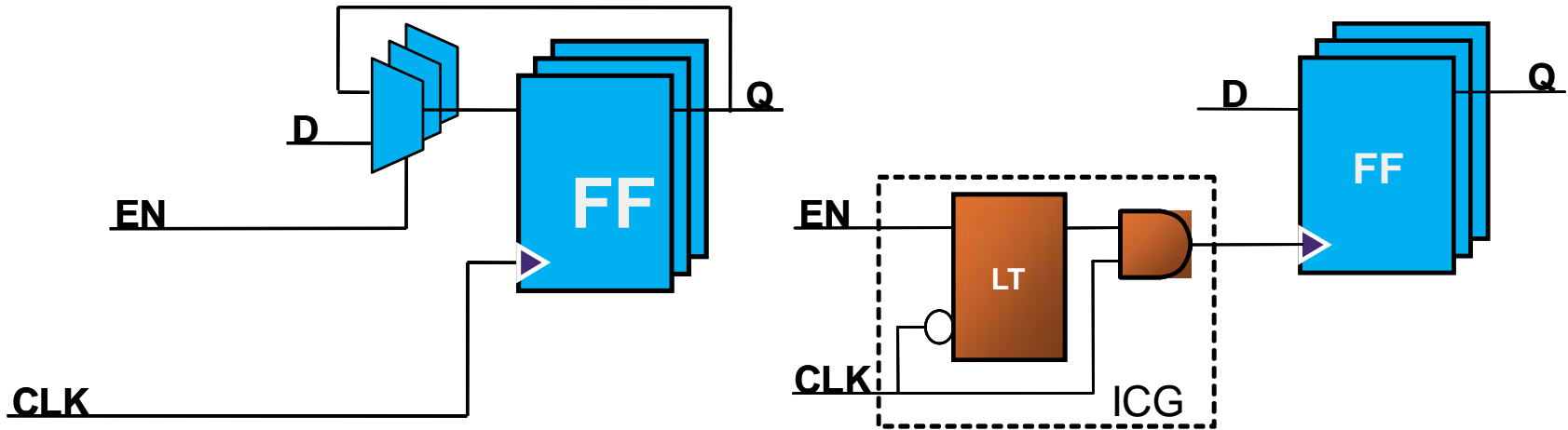


Stack Effect

Details on each Technique

- **Clock Gating**
 - Basic Understanding
 - Advantages
 - Concerns in the flow

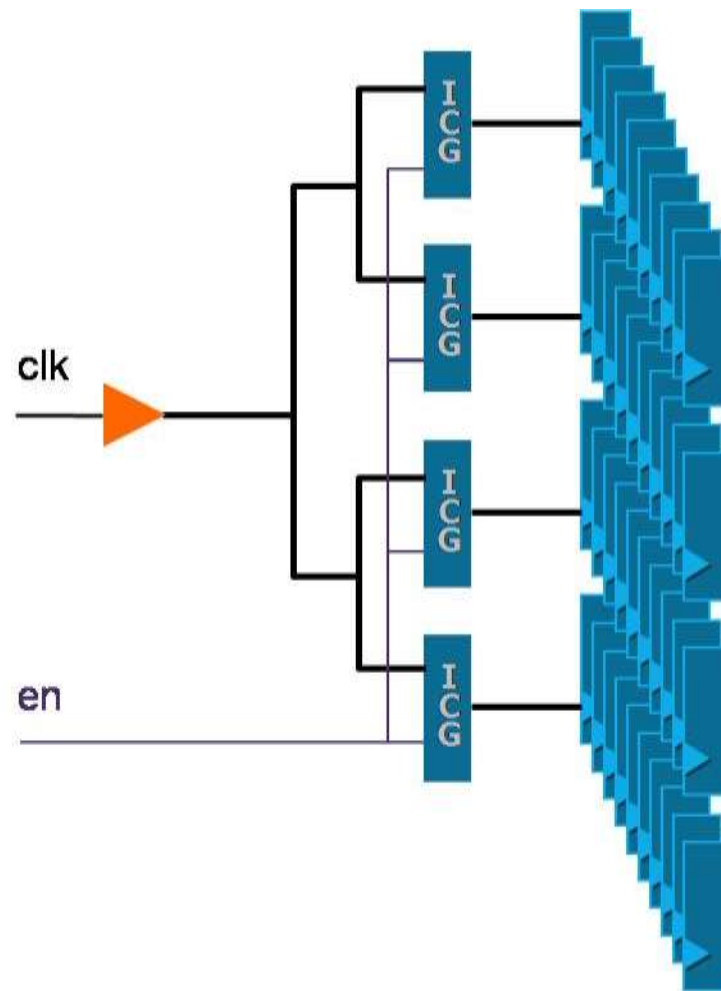
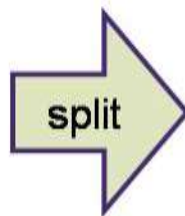
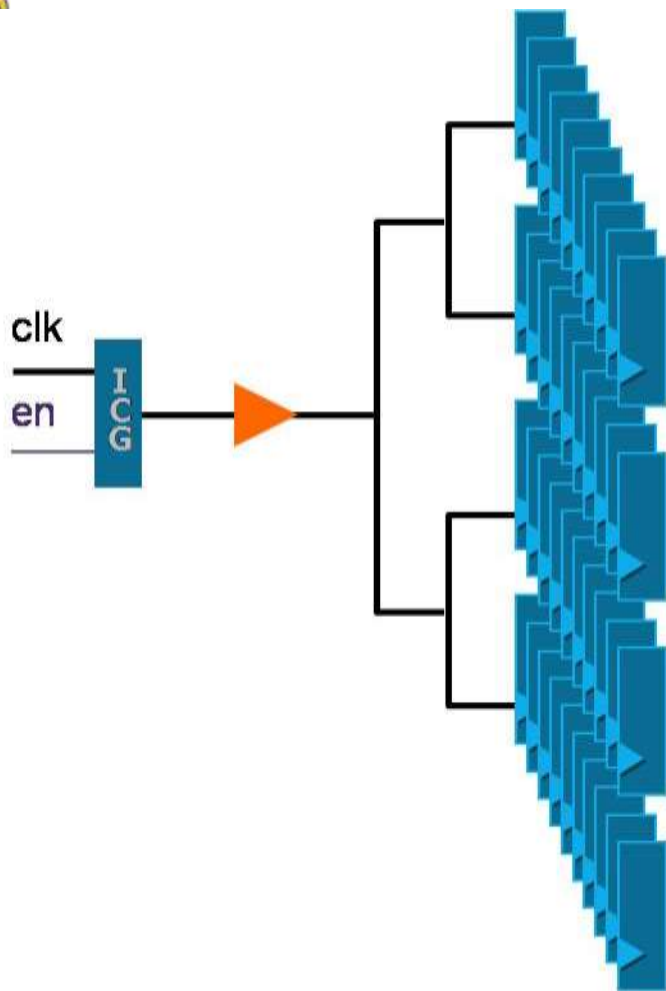
Understanding Clock Gating



Clock Gating Flow Challenges

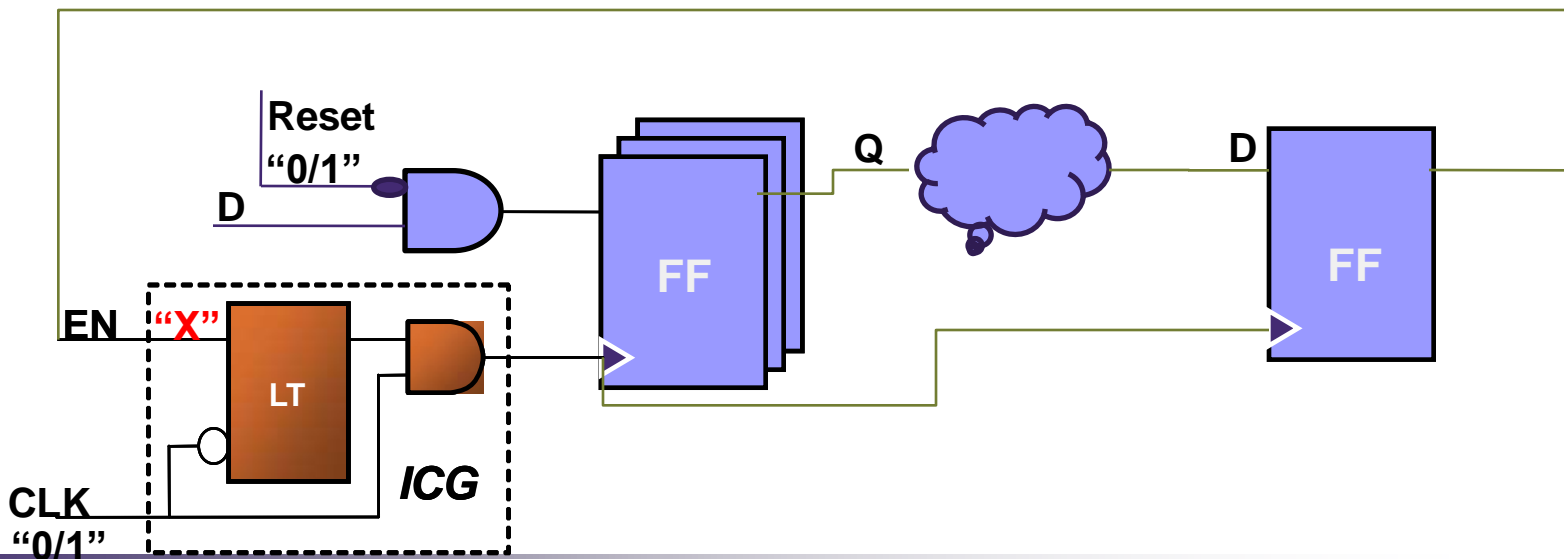
- Enable Timing
- Insertion delay increase
 - Impact on OCV
- Peak Power during ON/OFF of clock
 - IR drop as well
- Verification Impact

Managing Enable Timing



Clock Gating Impact on Verification

- RTL functional Simulation
 - None
- Gate level Simulation

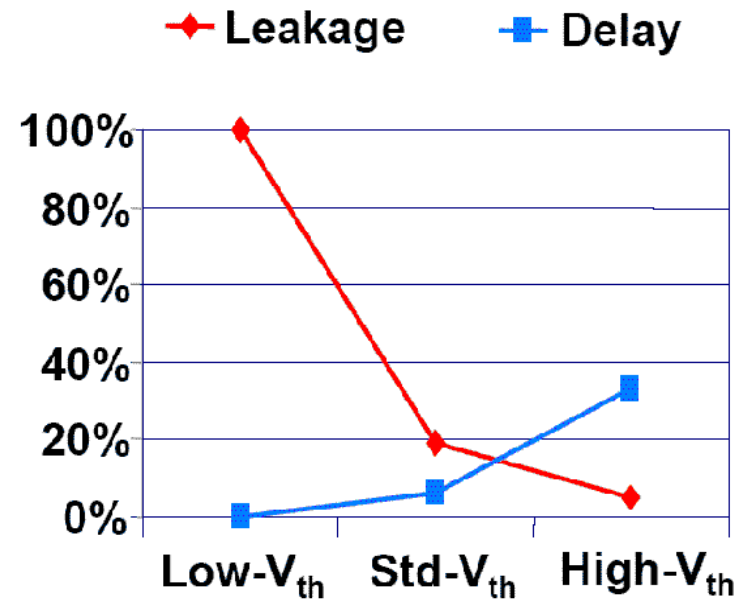
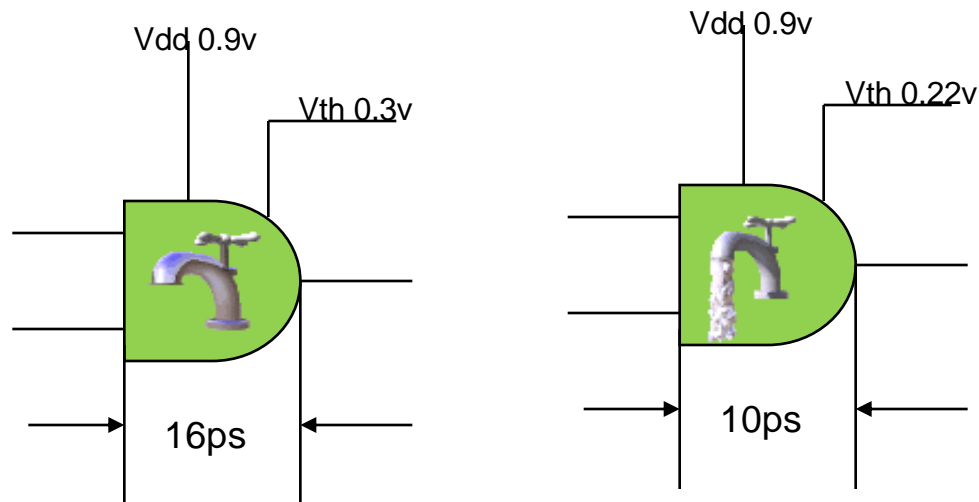


Details on each Technique

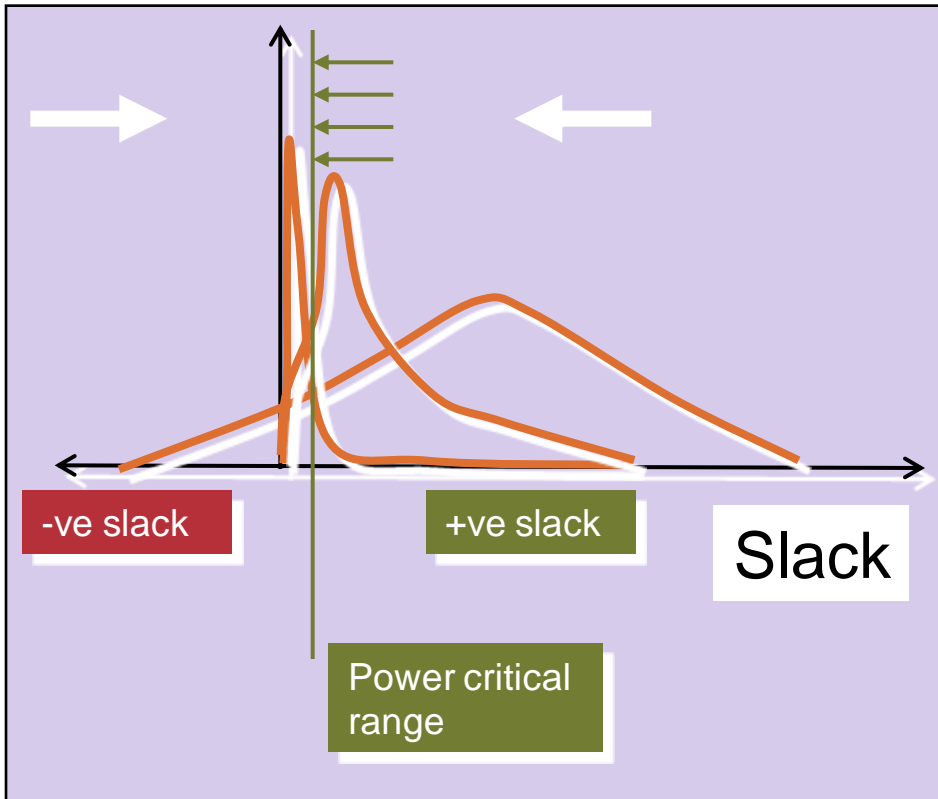
- **Multi-Threshold Leakage Optimization**
 - Basic Understanding
 - Advantages
 - Concerns in the flow

Understanding Multi Threshold

- Multiple Threshold Cells

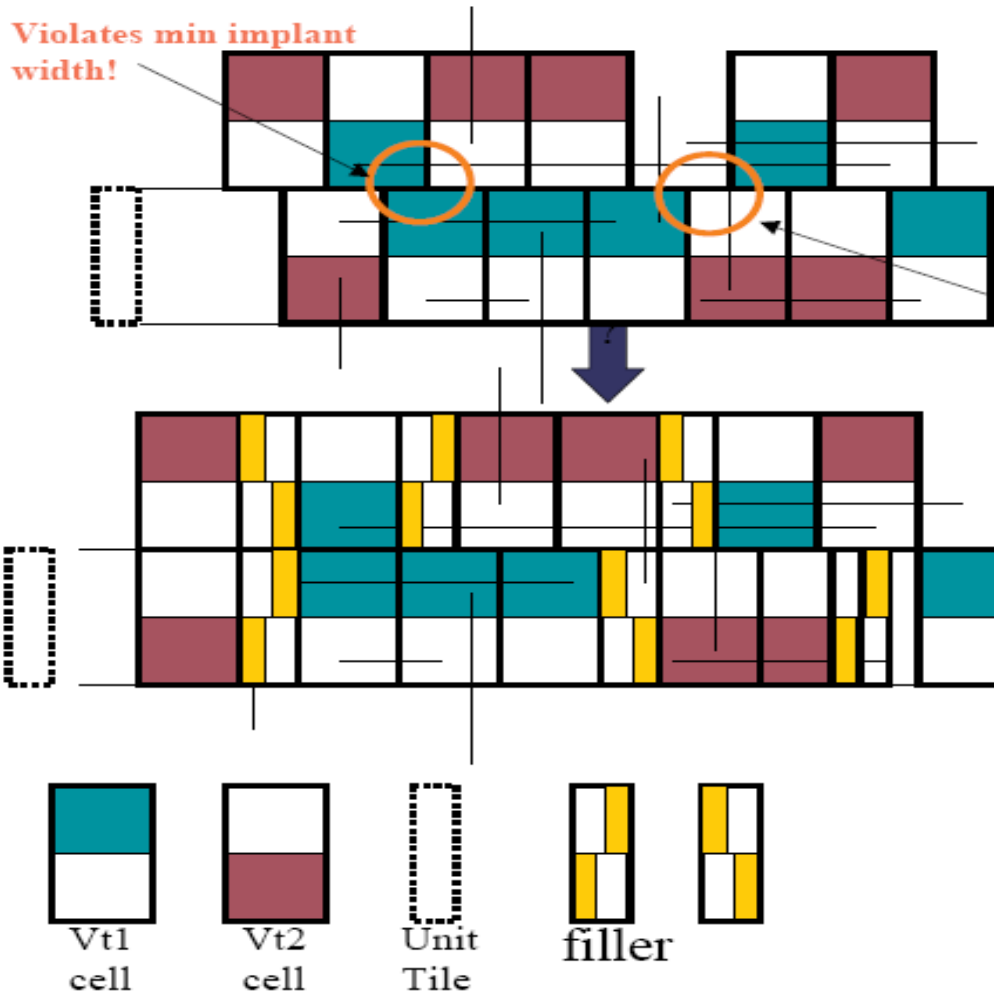


Multi-Threshold Flow Challenges



- Looking at a different view of the problem, optimizations push towards zero-slack
- High-Vt cells tend to be weaker and can be more susceptible to variability

Multi-Threshold Flow Challenges

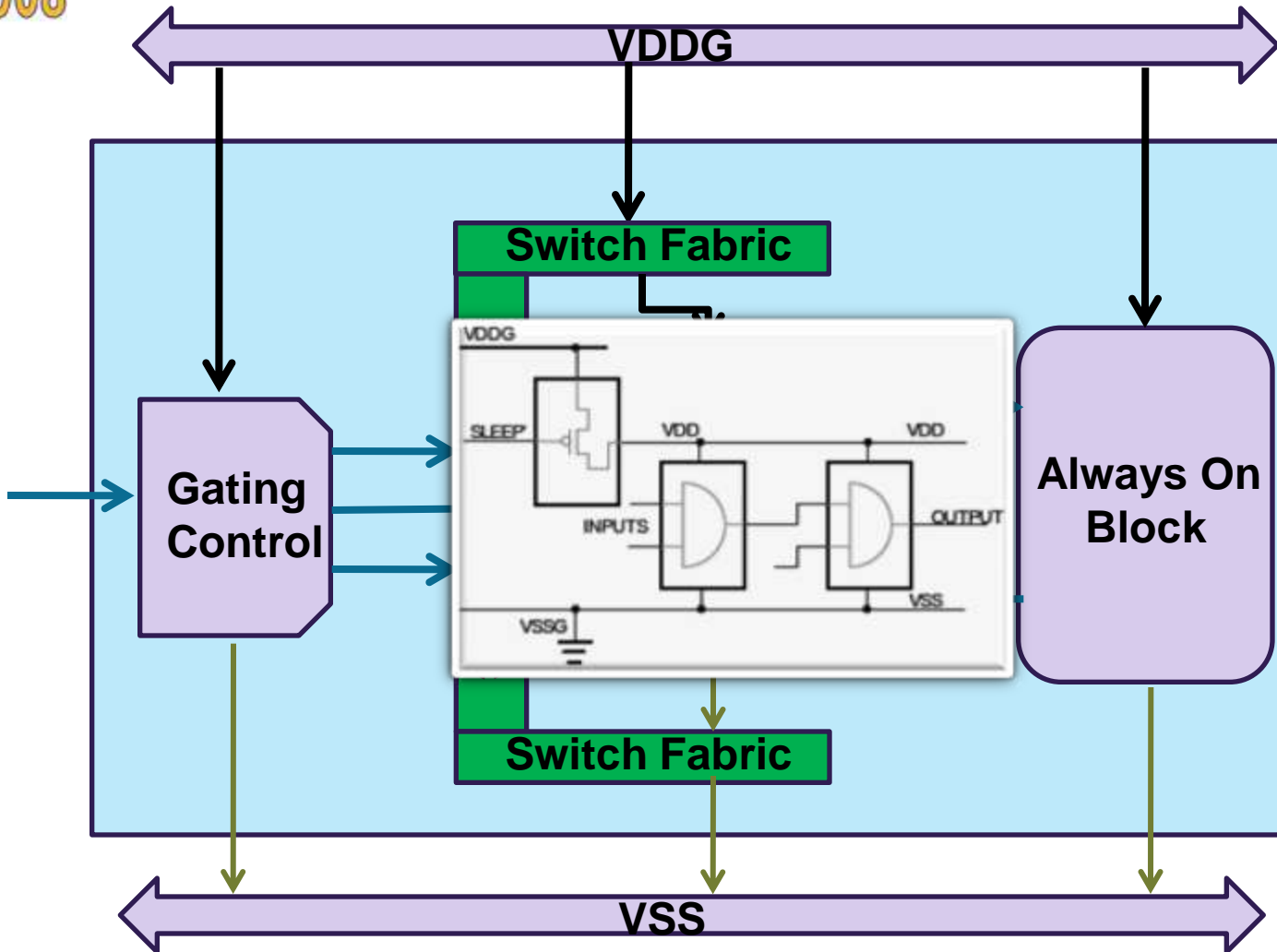


- Implant Spacing Violations
- Min Width Violations
- Chip Finishing requires Proper filler Cell Insertion

Details on each Technique

- **Power Gating**
 - Basic Understanding
 - Advantages
 - Concerns in the flow

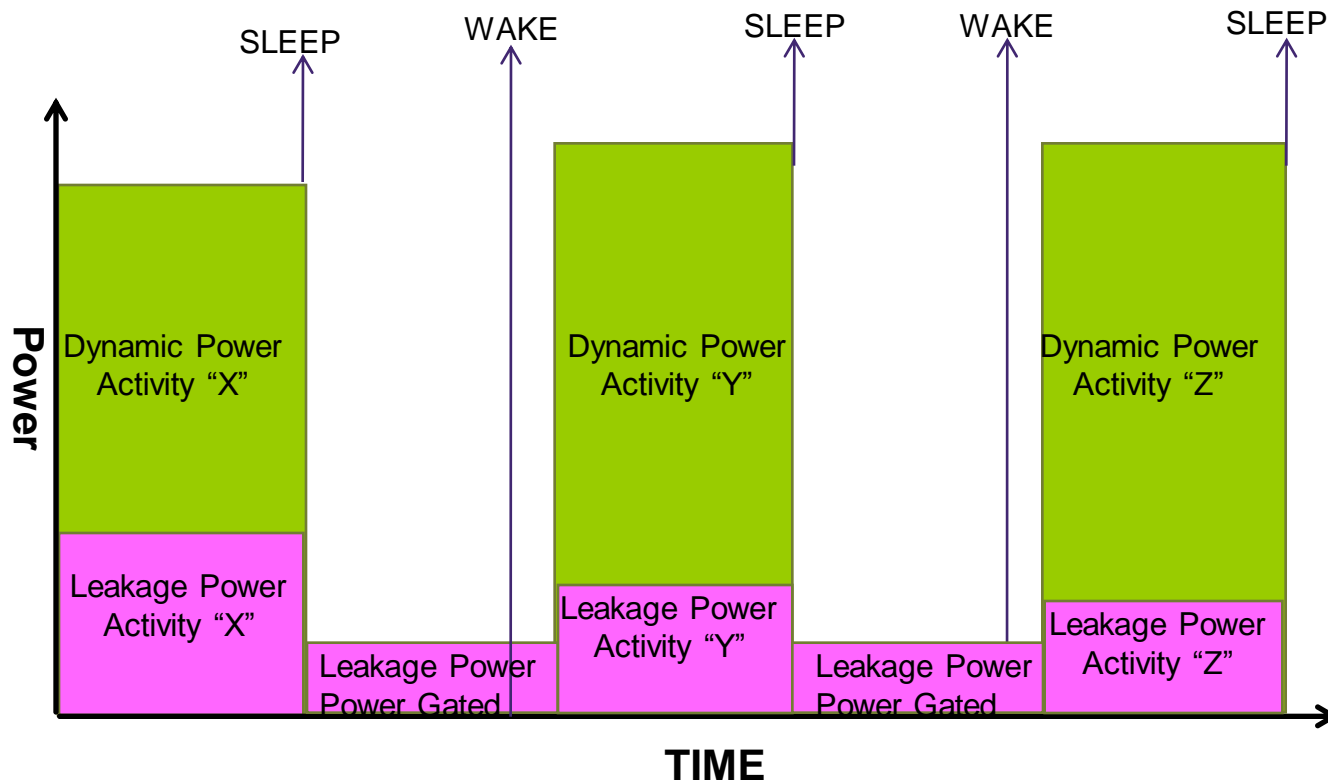
Understanding Power Gating



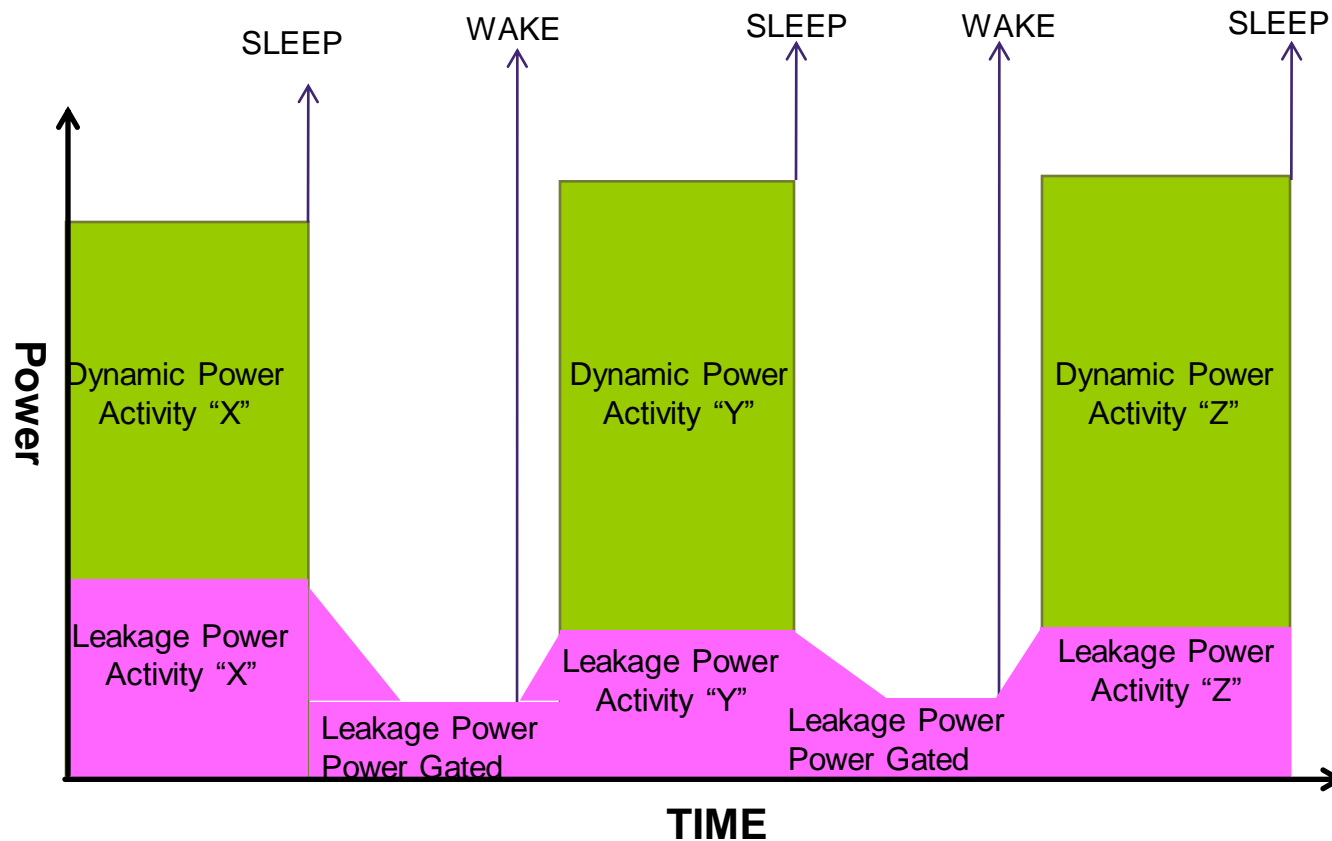
Architectural Tradeoffs

- Amount of leakage power savings that is possible
- Entry and exit time penalties incurred
- Energy dissipated entering and leaving such leakage saving modes

Activity Profile for Power Gating

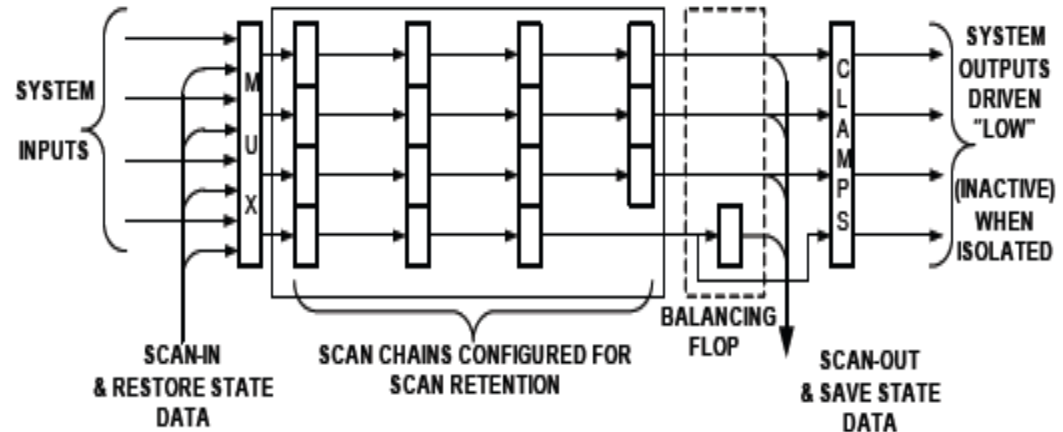
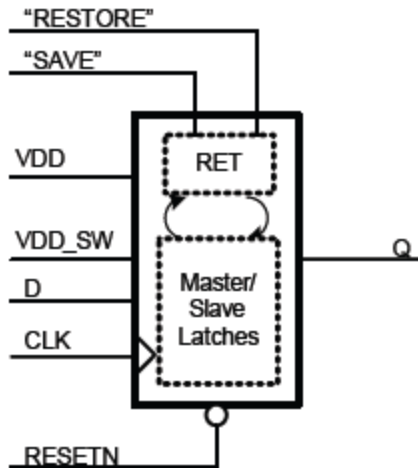
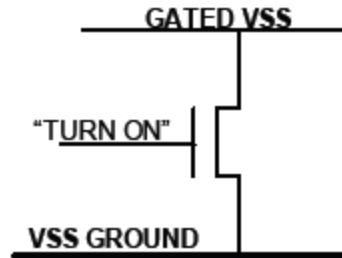
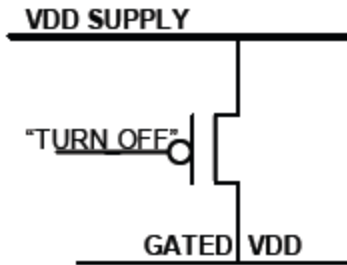


Realistic Profile for Power Gating



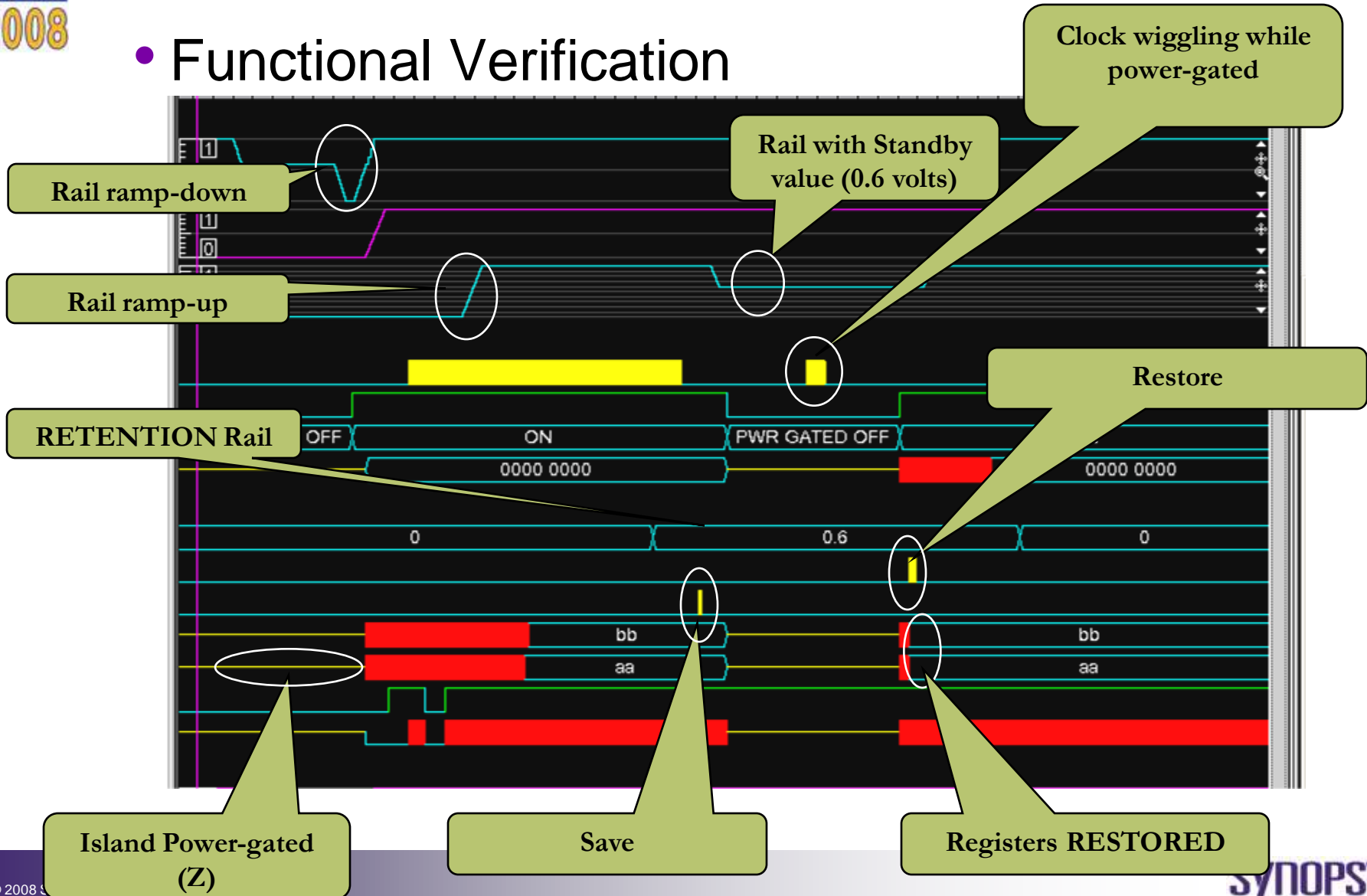
Architectural Tradeoffs

- Gate VDD or VSS?
- Retention Mechanism



Power Gating Flow Challenges

- Functional Verification

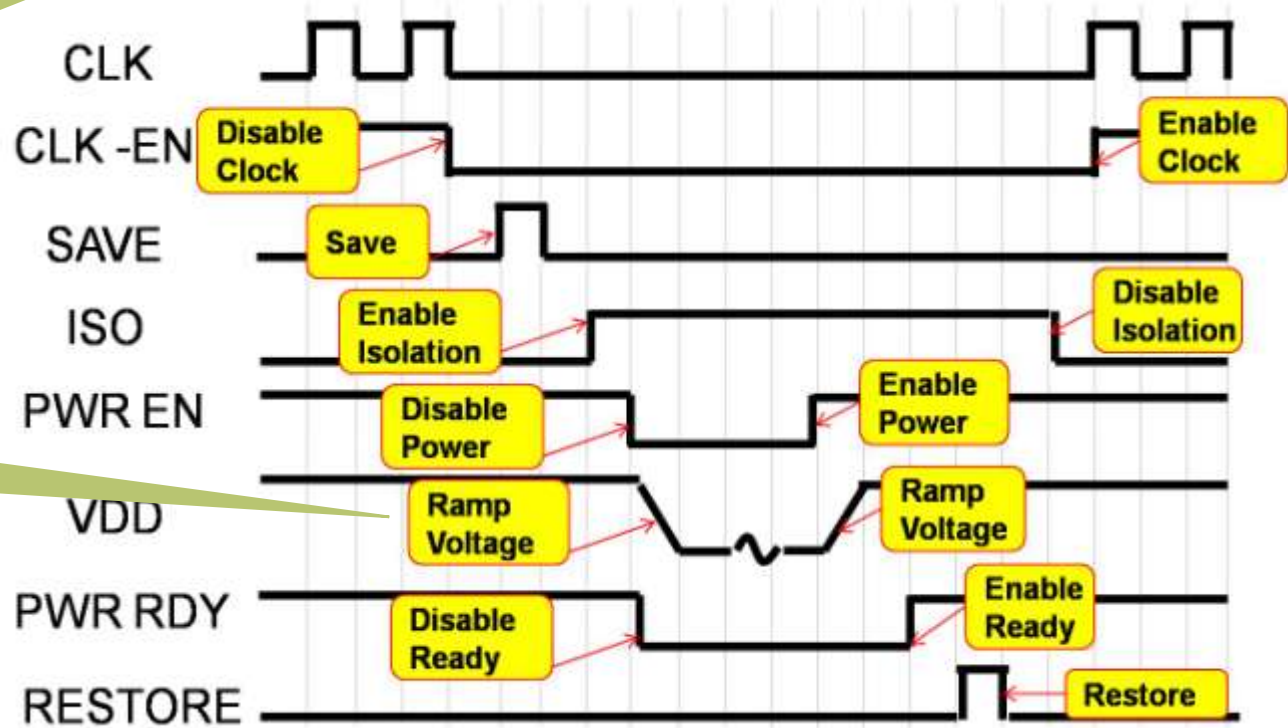


Power Gating Sequence/Coverage

MV FSM	Sequence	Toggles	Testbench Grader	Assertion	Summary			
MV FSM			Voltage State	Logical State	Transitions	All States	Sequences	
OCP			Coverage	8/8	2/3	8/17	10/11	4/6

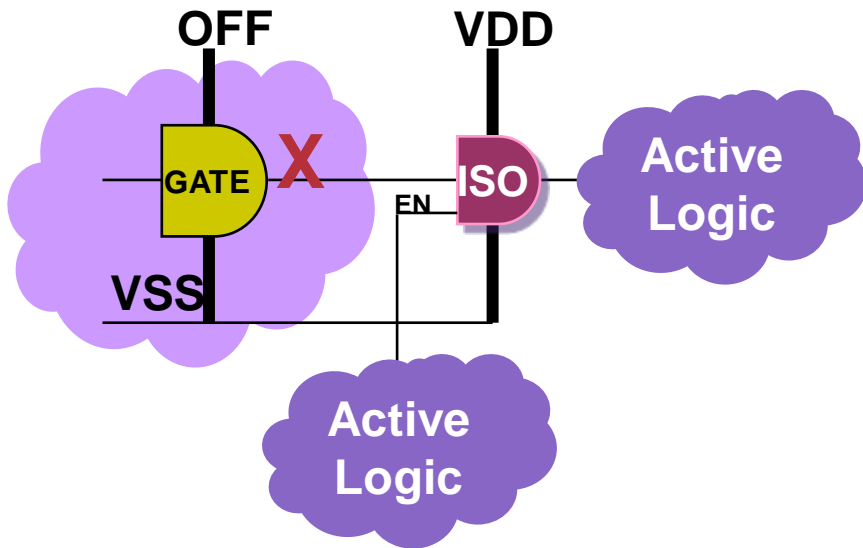
Voltage States: 8/8
Logical States: 2/3

Is the wakeup/shutdown sequence correct ?

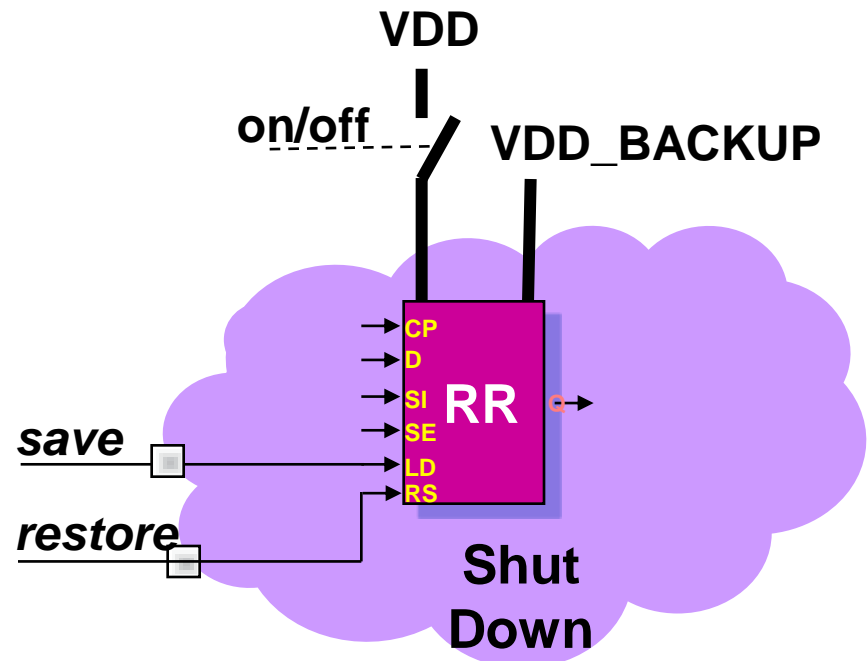


Power Gating Flow Challenges

- Logic Synthesis



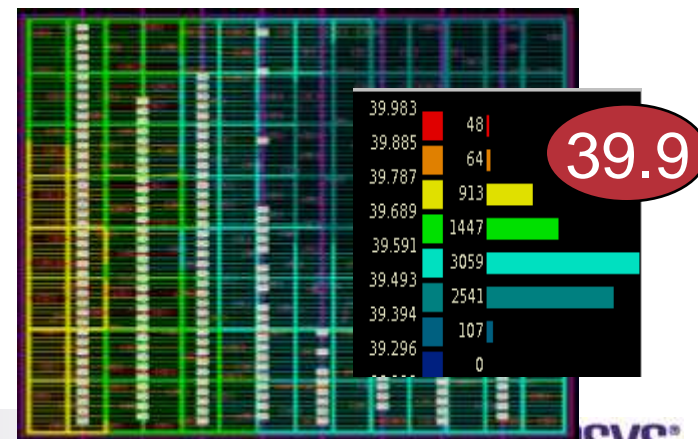
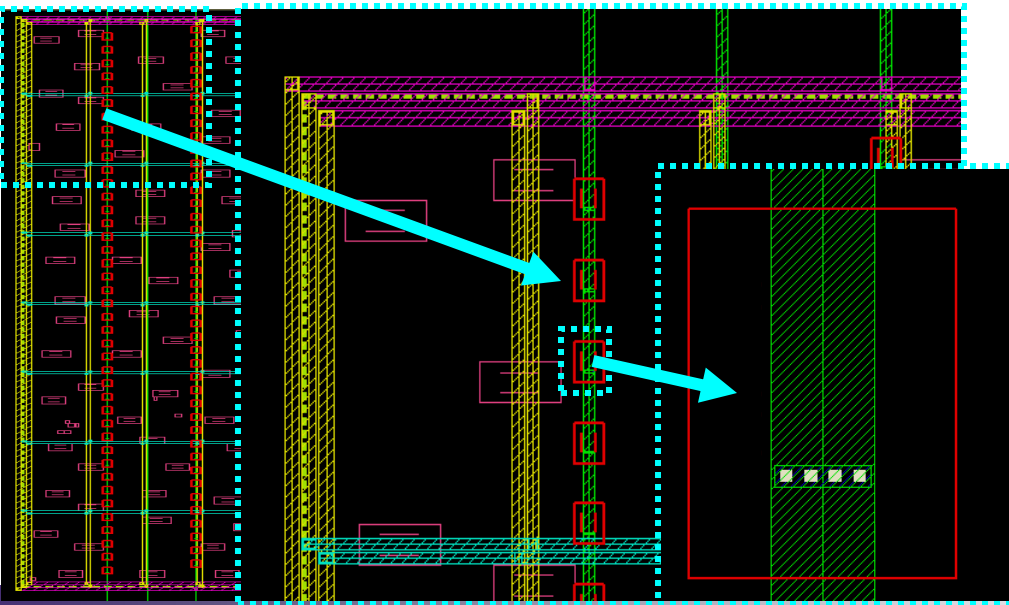
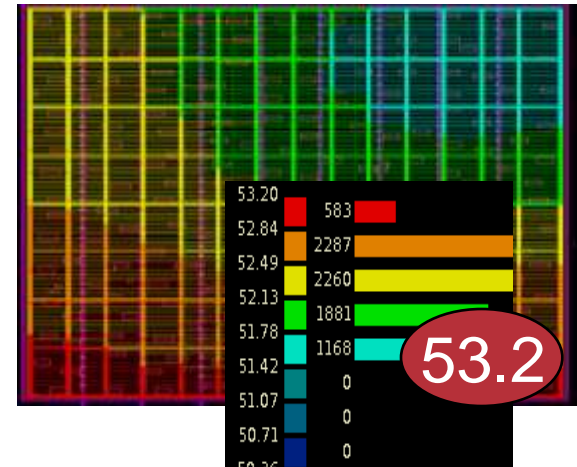
Insert Isolation Cell



Insert Retention Register
Hookup Retention Register

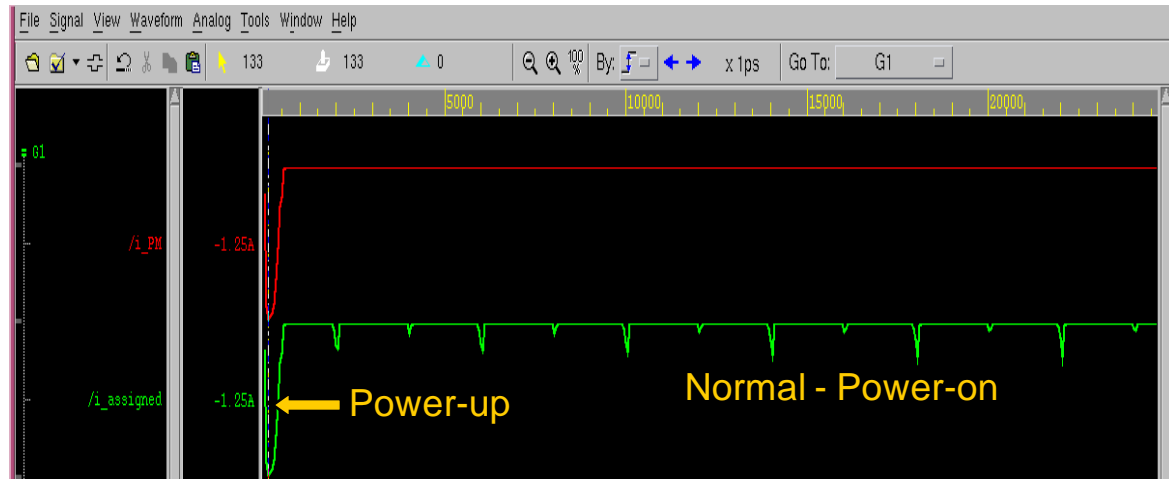
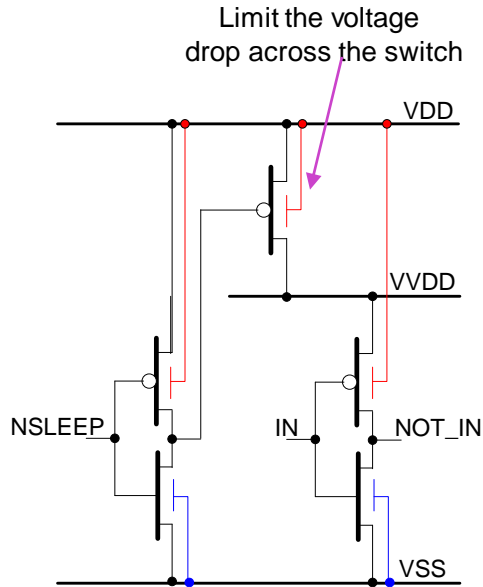
Power Planning the Switches

MAXIR (mV)	Area (%)	Resistance	# PWR SWITCHES	X_INCR	Y_INCR	LIB_CEL_NAME
37.2	0.4	650.0	328.0	26.3	3.6	SXXZZYX8L
42.7	0.3	1300.0	328.0	26.3	3.6	SXXZZYX4L
43.6	0.2	650.0	164.0	26.3	7.2	SXXZZYX8L
53.2	0.2	2600.0	328.0	26.3	3.6	SXXZZYX2L
55.3	0.2	1300.0	164.0	26.3	7.2	SXXZZYX4L
72.5	0.2	650.0	164.0	52.6	3.6	SXXZZYX8L

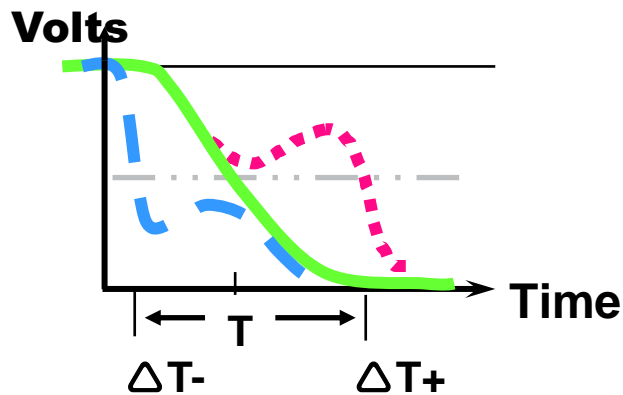
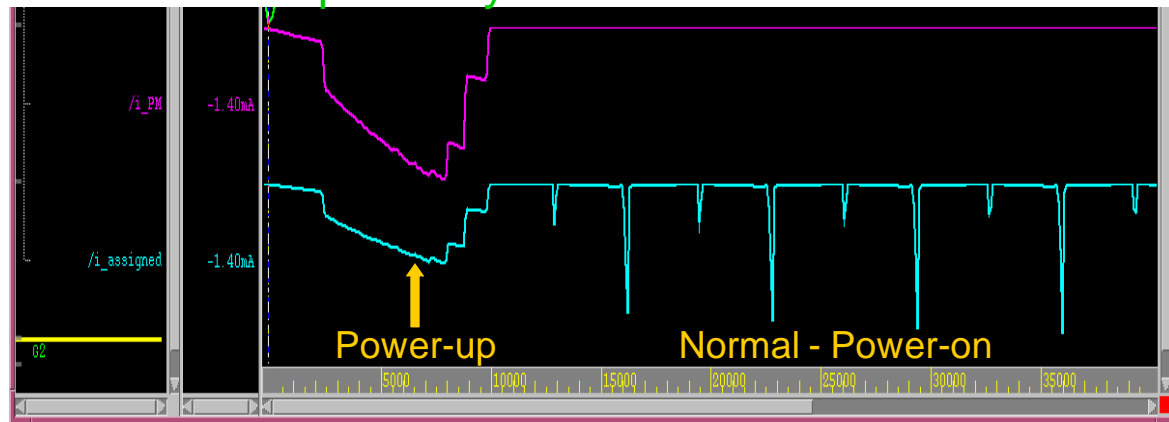


IR-Drop Management

Turn On All Switches at Once



Sequentially Turn On Switches

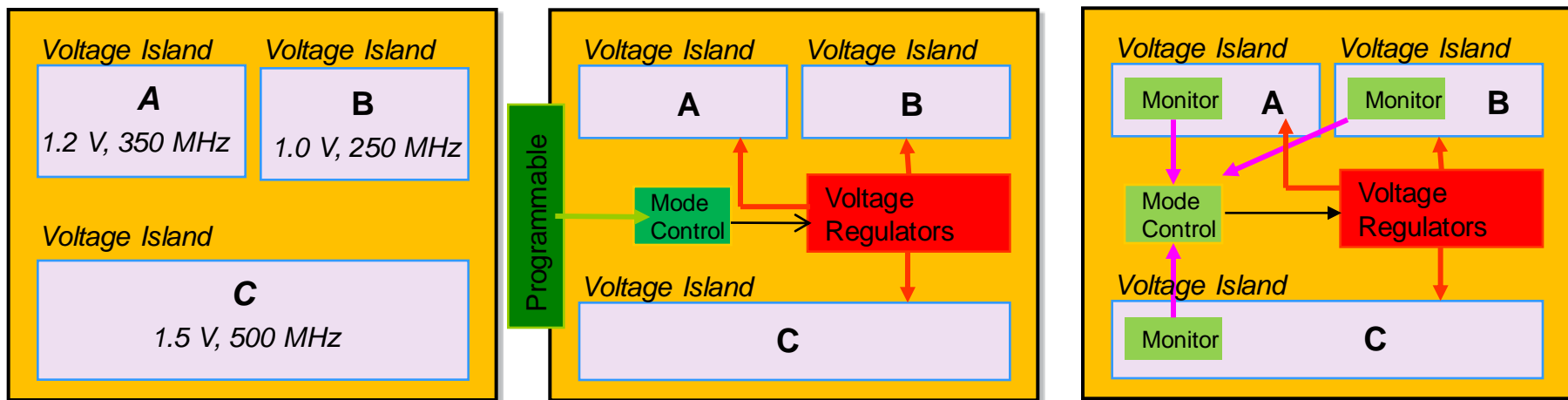


Details on each Technique

- **Multi-Voltage**
 - Basic Understanding
 - Advantages
 - Concerns in the flow

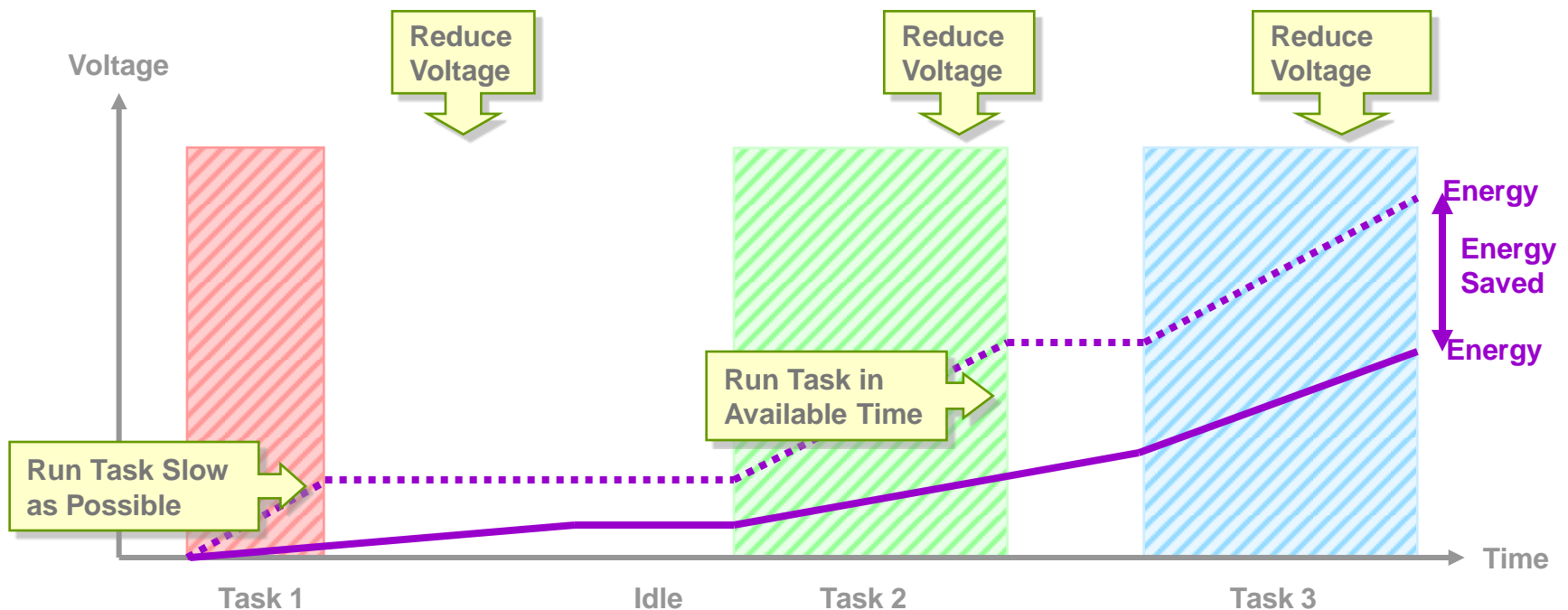
Multi-Voltage Design Style

- Static Voltage
- Multi-Level Voltage Scaling
- Dynamic Voltage and Frequency Scaling
- Adaptive Voltage Scaling

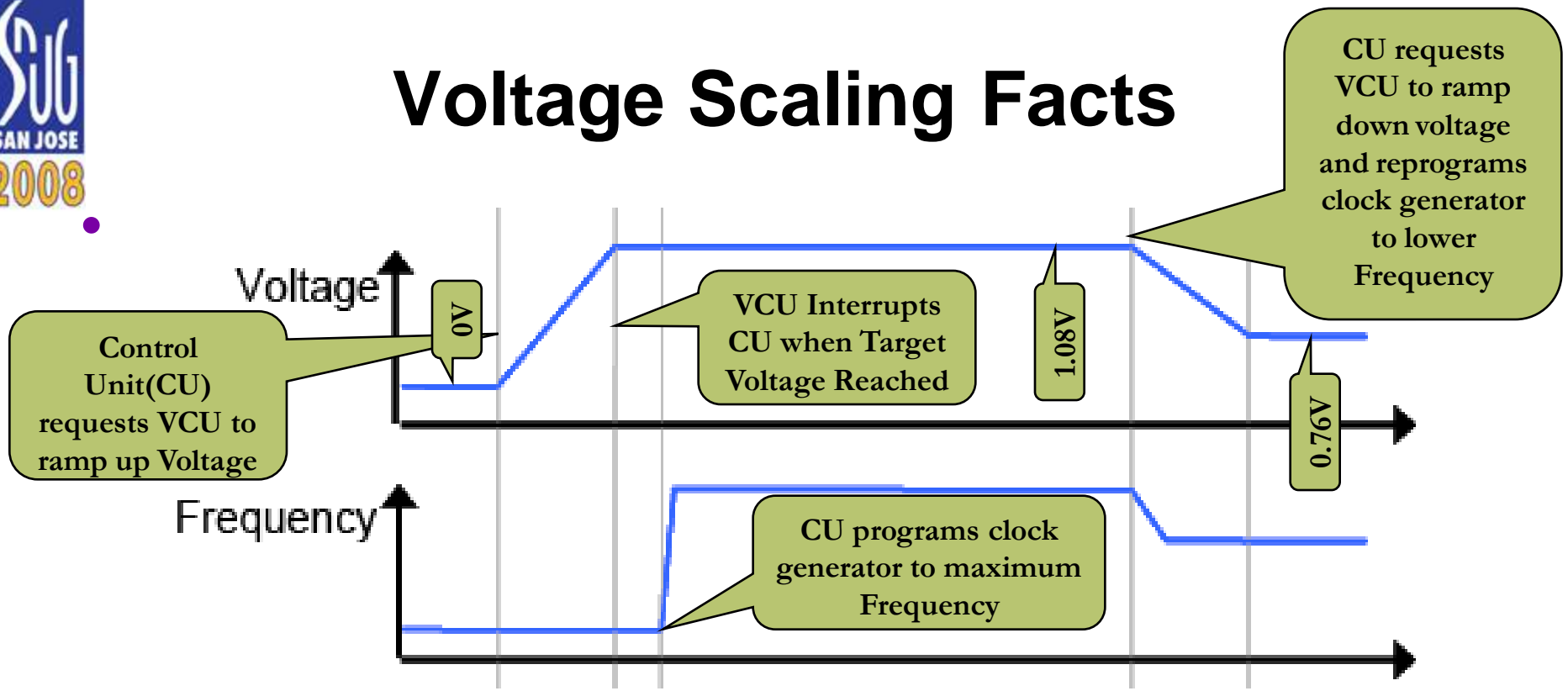


Understanding Multi-Voltage/Scaling

- Avoid completing tasks early – energy is wasted
- Use only enough energy required to complete task in time



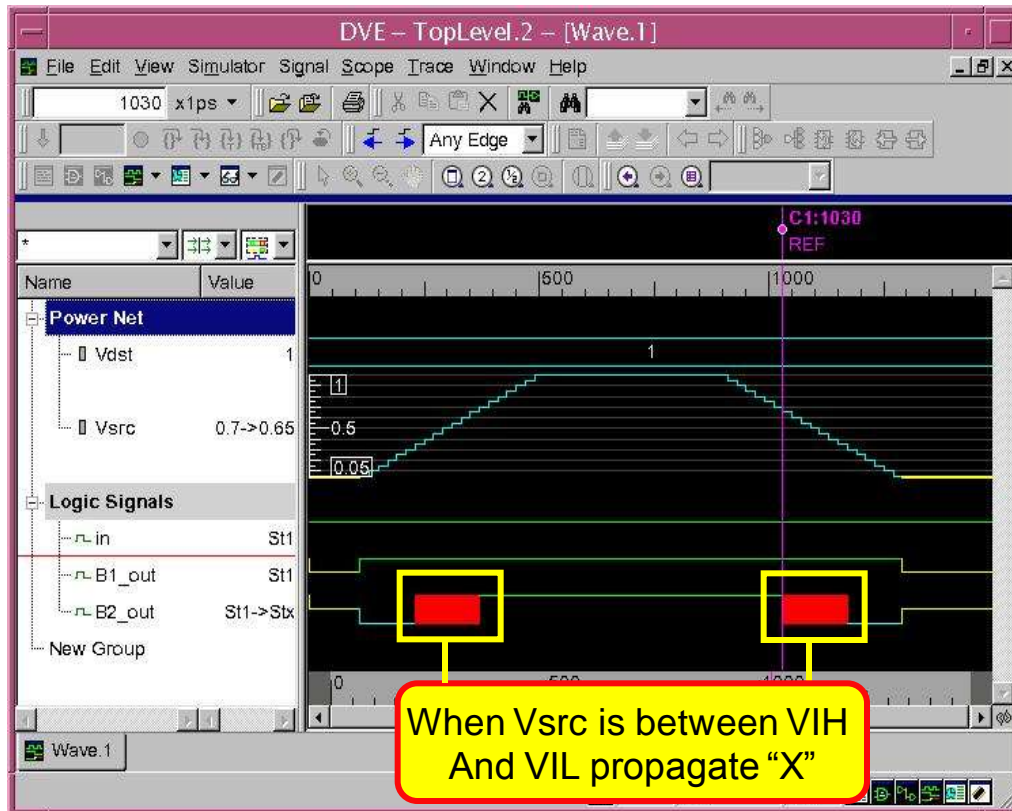
Voltage Scaling Facts



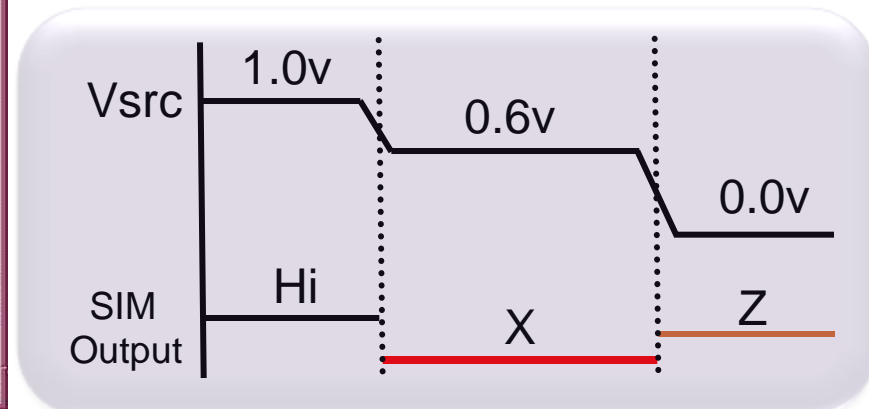
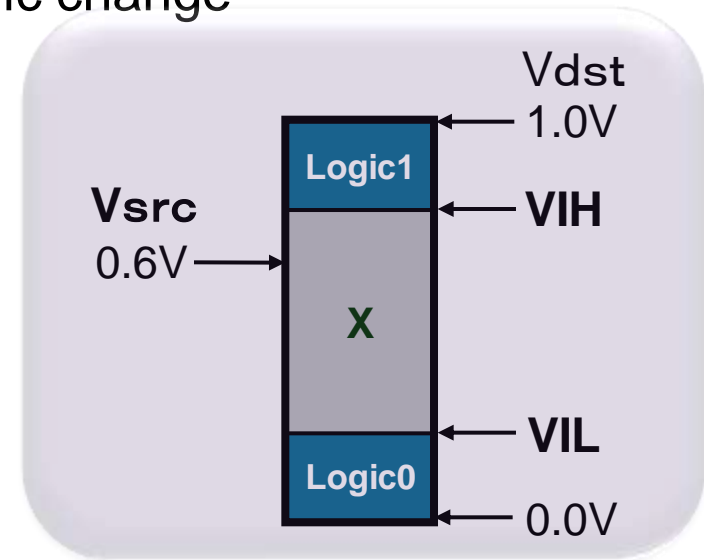
- Identify the various operating voltages under which blocks will be operating at any point of time
- Do we have libraries characterized at these V points?

Voltage Scaling Flow Challenges

- Accurately represent effects of dynamic change in voltage values during simulation

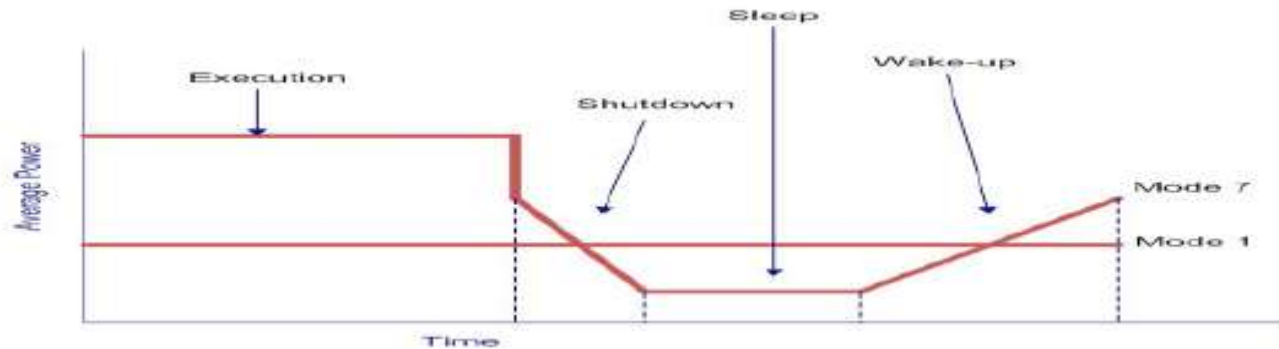


When Vsrc is between VIH And VIL propagate "X"

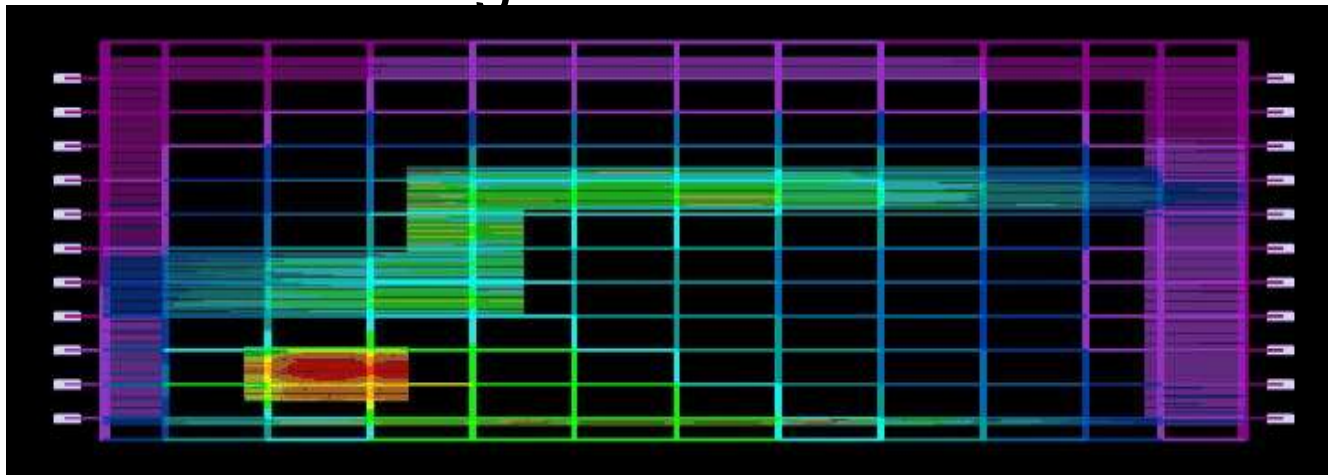


Voltage Scaling Flow Challenges

- Synthesis

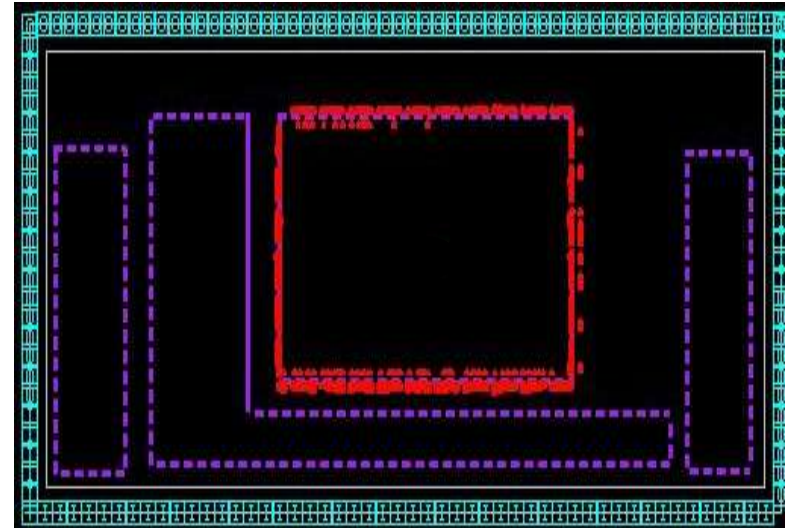


- Power Planning

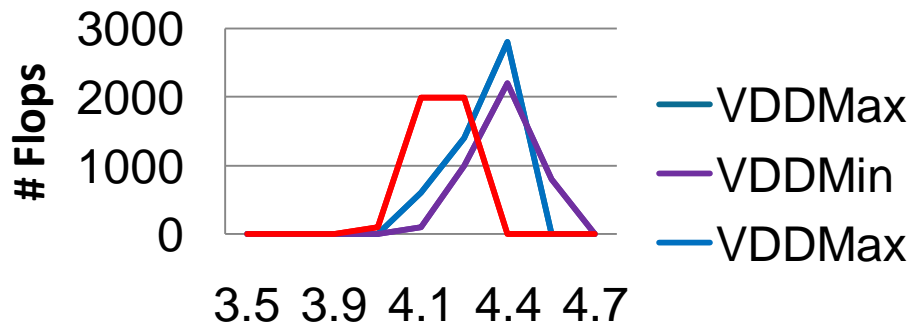


Voltage Scaling Flow Challenges

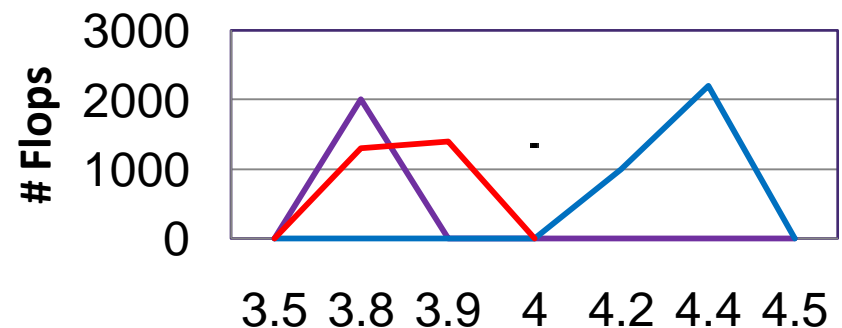
- Placement, CTS and Route
 - Minimize Skew
 - MCM
 - Placement of Level Shifters
 - Temperature Inversion



Reduced Skew Across Domains

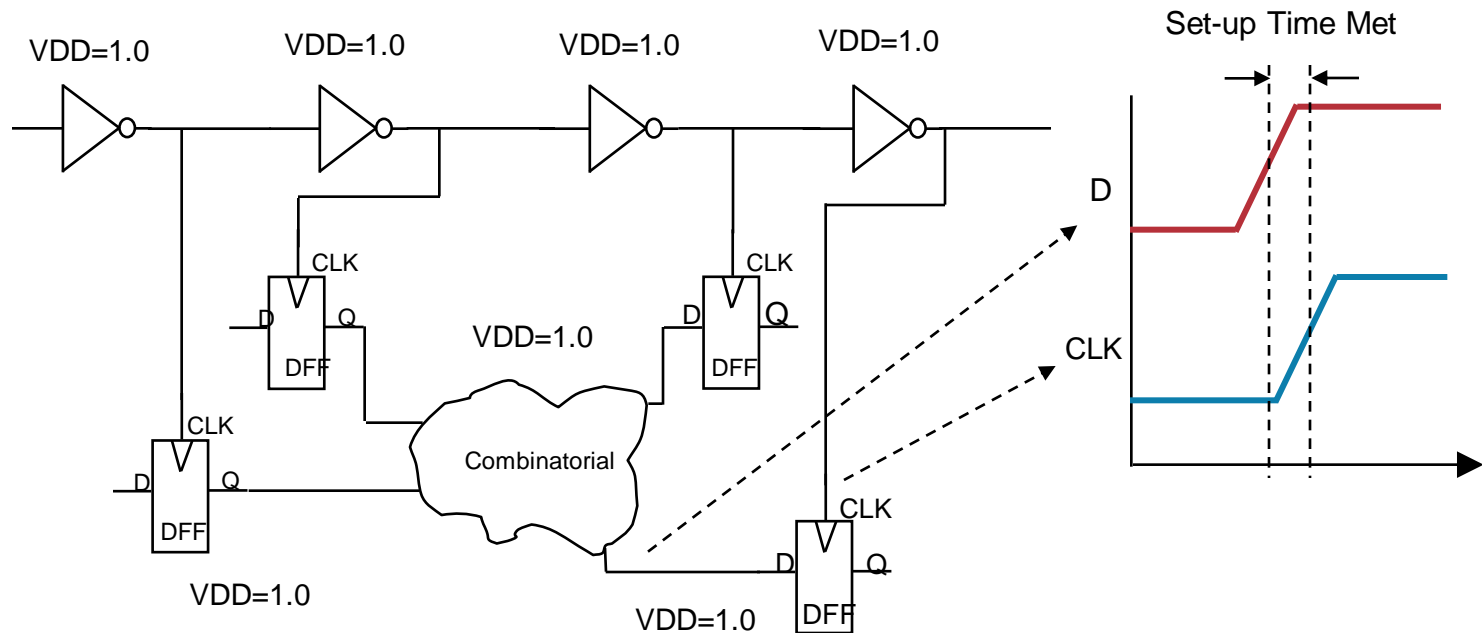


Large Skew Across Domains



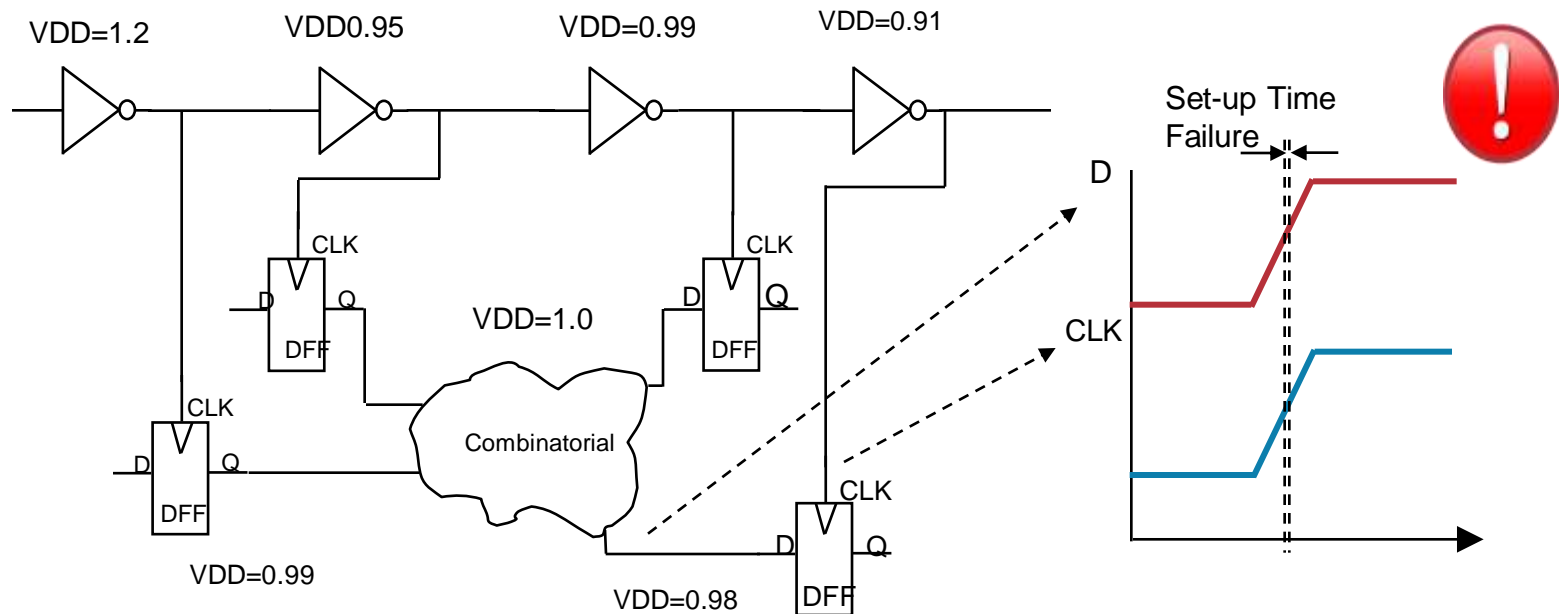
Voltage Scaling Timing Challenges

- Functional or Performance Failures



Voltage Scaling Timing Challenges

- Functional or Performance Failures

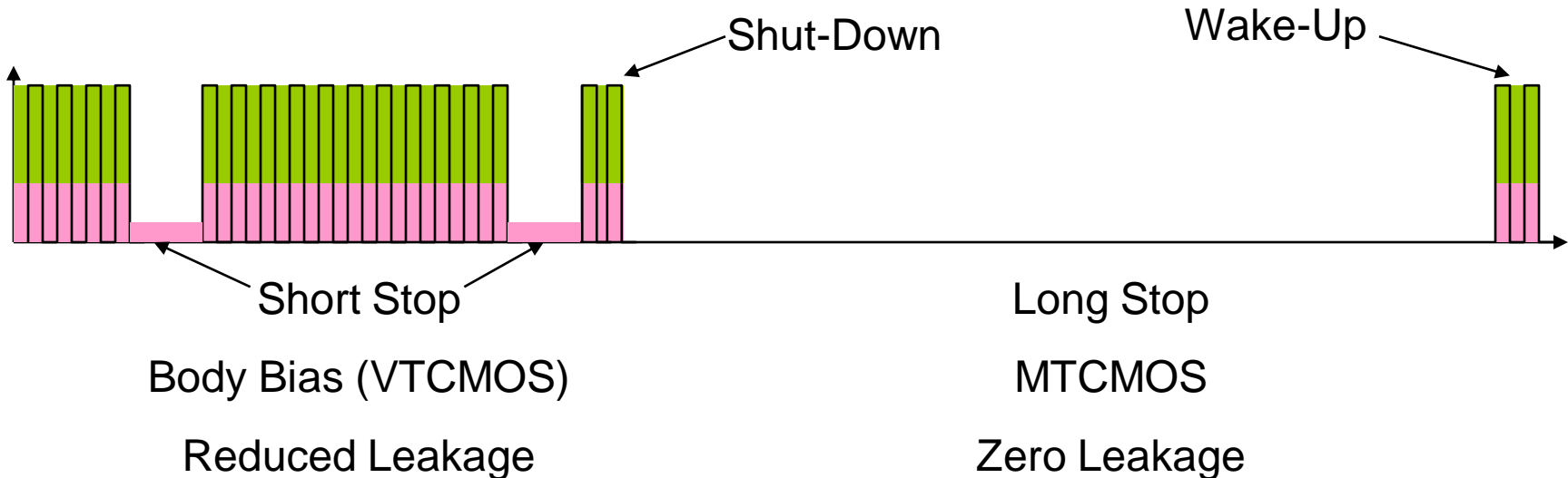
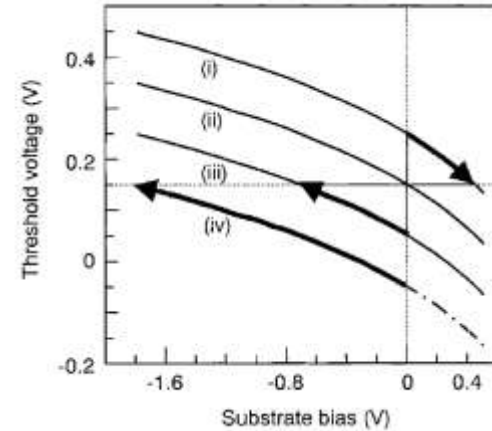
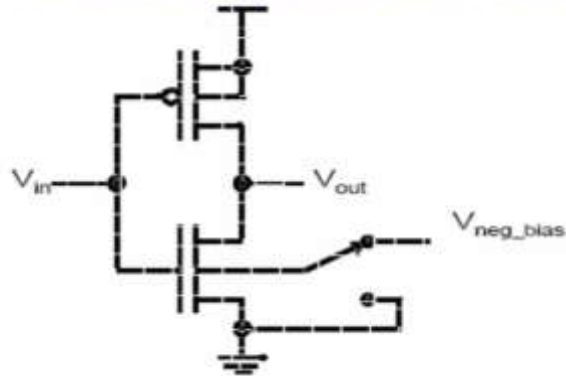


Details on each Technique

- **Back Biasing**
 - Basic Understanding
 - Advantages
 - Concerns in the flow

Understanding Biasing

VTCMOS (Variable V_{TH} CMOS)



Body Bias (VTCMOS)

Reduced Leakage

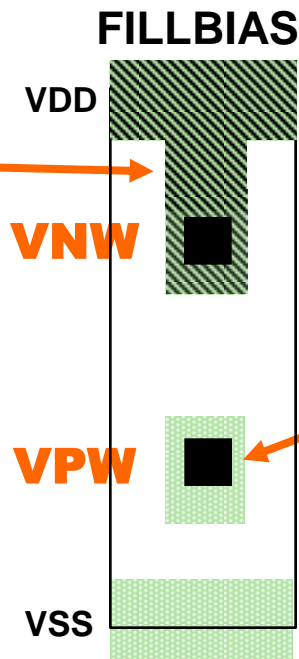
Long Stop

MTCMOS

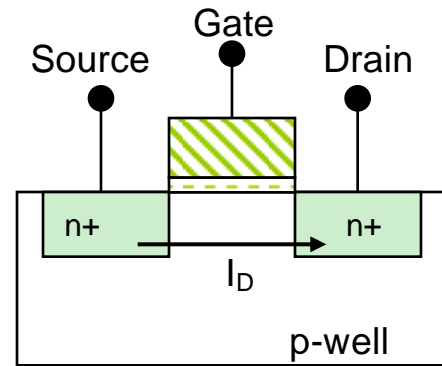
Zero Leakage

Reducing Leakage using Well Bias

Connect N-Well to VDD

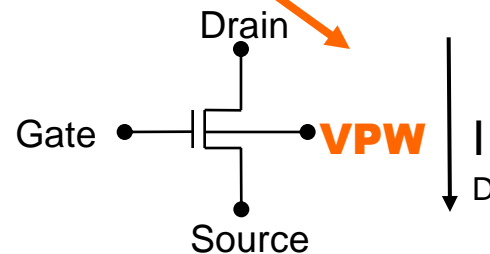


Connect P-Well to VSS - 0.3V



VPW

- When **VPW** < Source
 - V_{th} increases
 - I_D decreases
- Leakage **decreases**



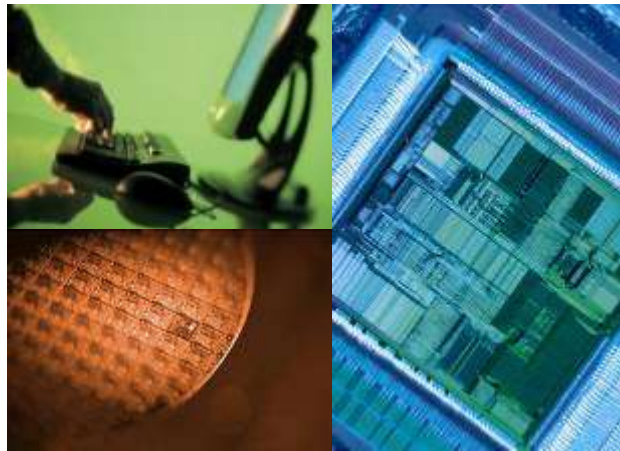
Well Biasing Flow Challenges

- Impact on Area due to extra Pick-Up cells
- Multi-Corner Analysis required for Sign-Off
 - $V_{BB} = 1V$, $V_{BB} = 2V$...etc
- Sleep to Transition Power Overhead
- LVS complexity
- Well RC extraction

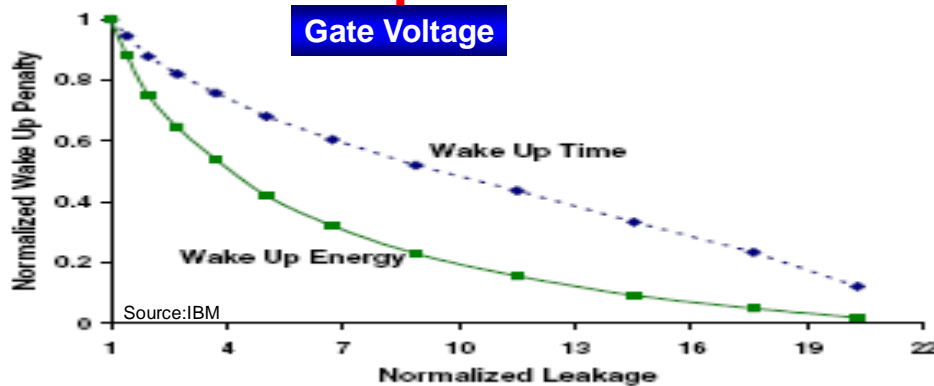
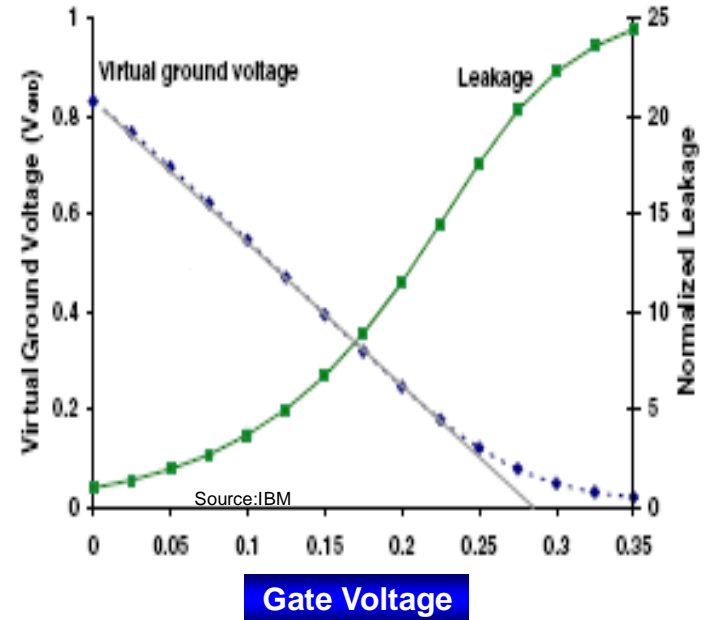
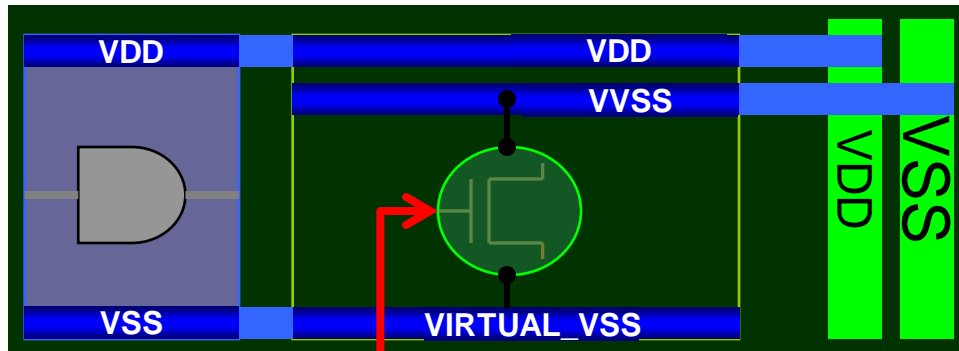
Power Savings Data

Technique Used	Technology	% Leakage Savings	% Total Power Savings
Clock gating	90nm	NA	57%
Multi-Vt	90nm	31%	NA
Power Gating	130nm	25X	13x
Power Gating	65nm	2x	NA
DVFS	45nm	98% during Standby	NA

Thoughts on Efficient Leakage Power Management



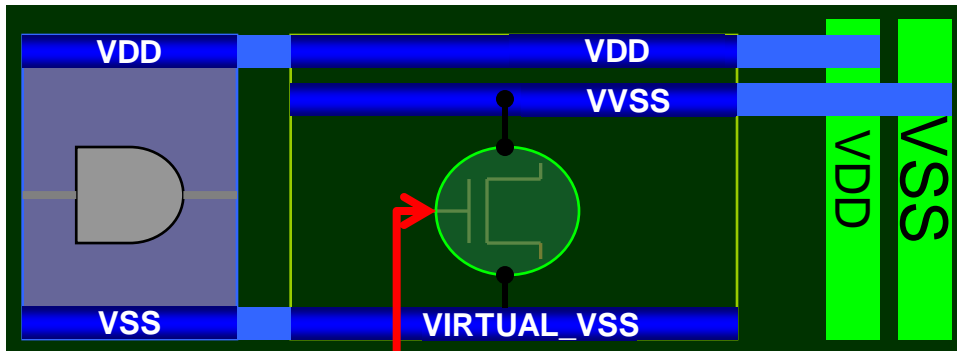
Efficient Leakage Power Management



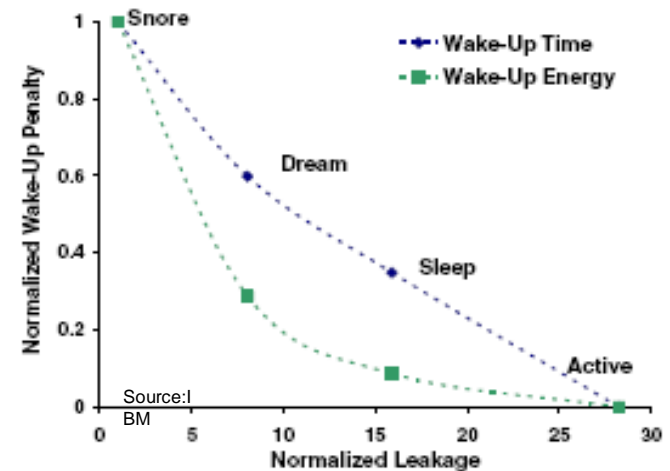
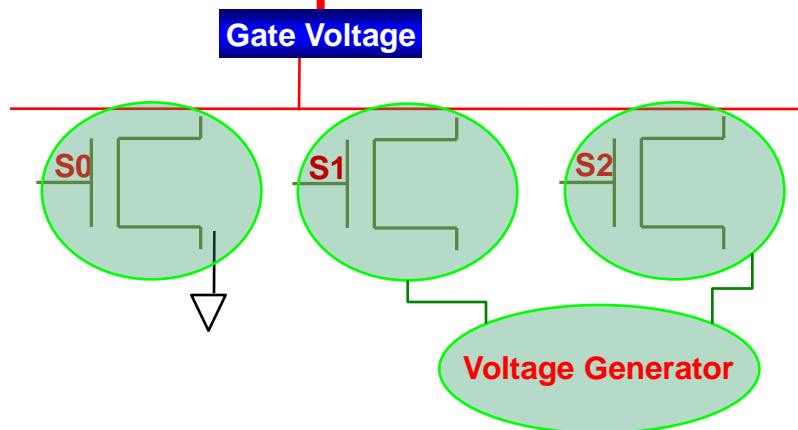
Gate Voltage

Gate Voltage

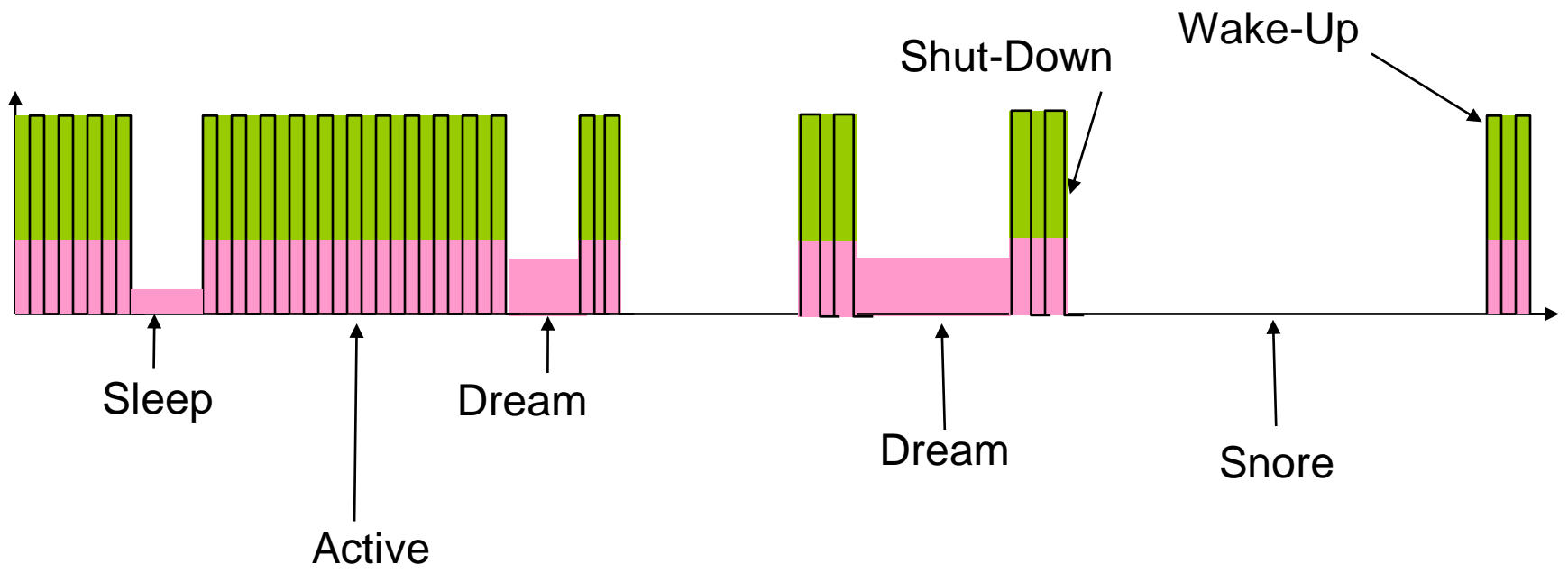
Multiple Power Mode Implementation



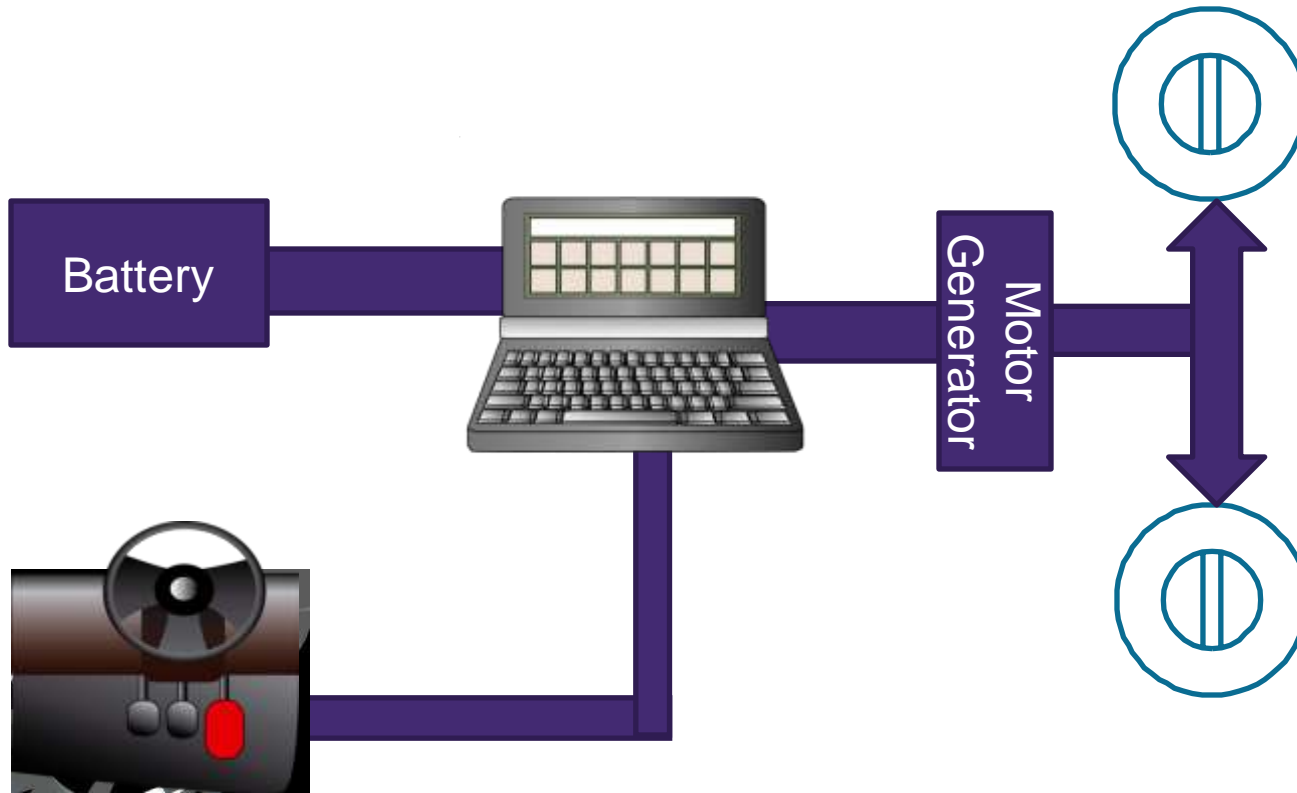
S0	S1	S2	
1	0	0	Snore
0	1	0	Dream
0	0	1	Sleep
0	1	1	Active



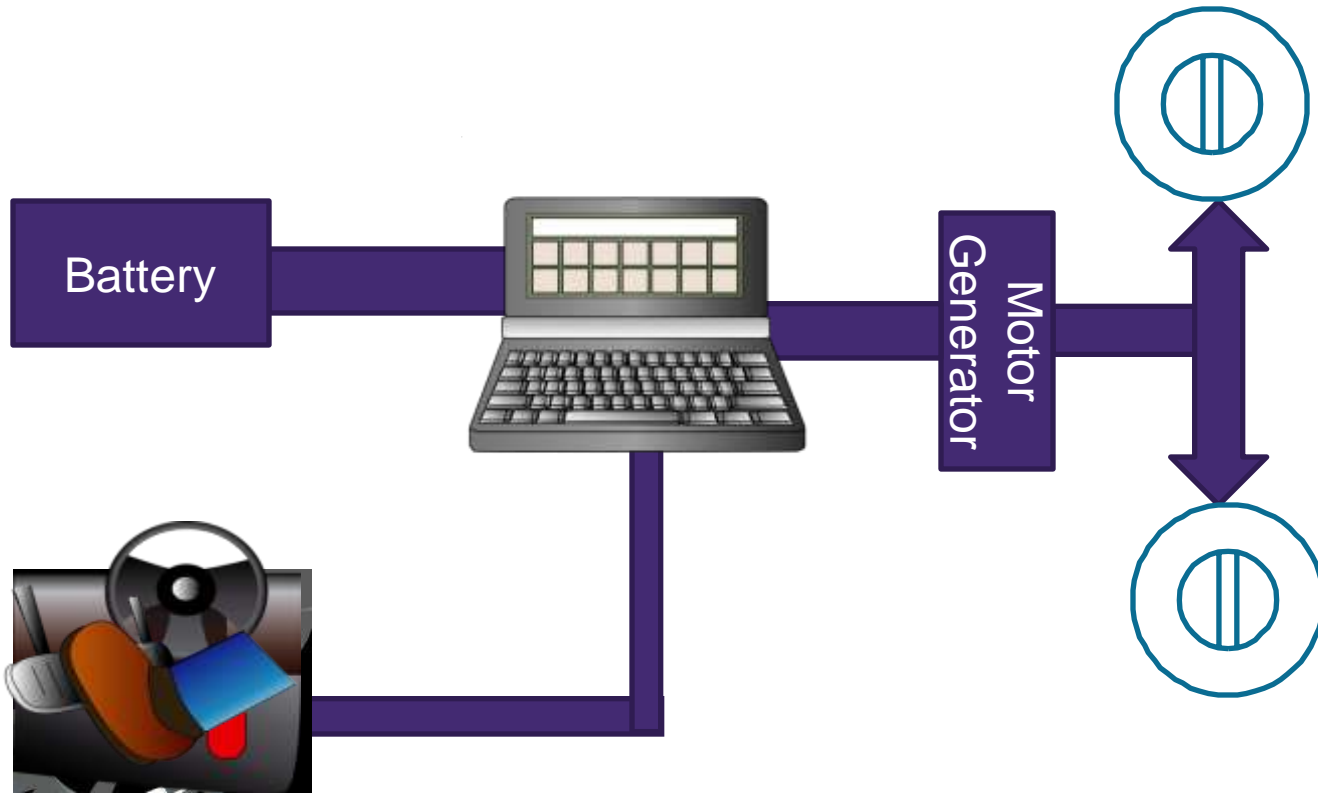
Activity Profile of Multiple Sleep Modes



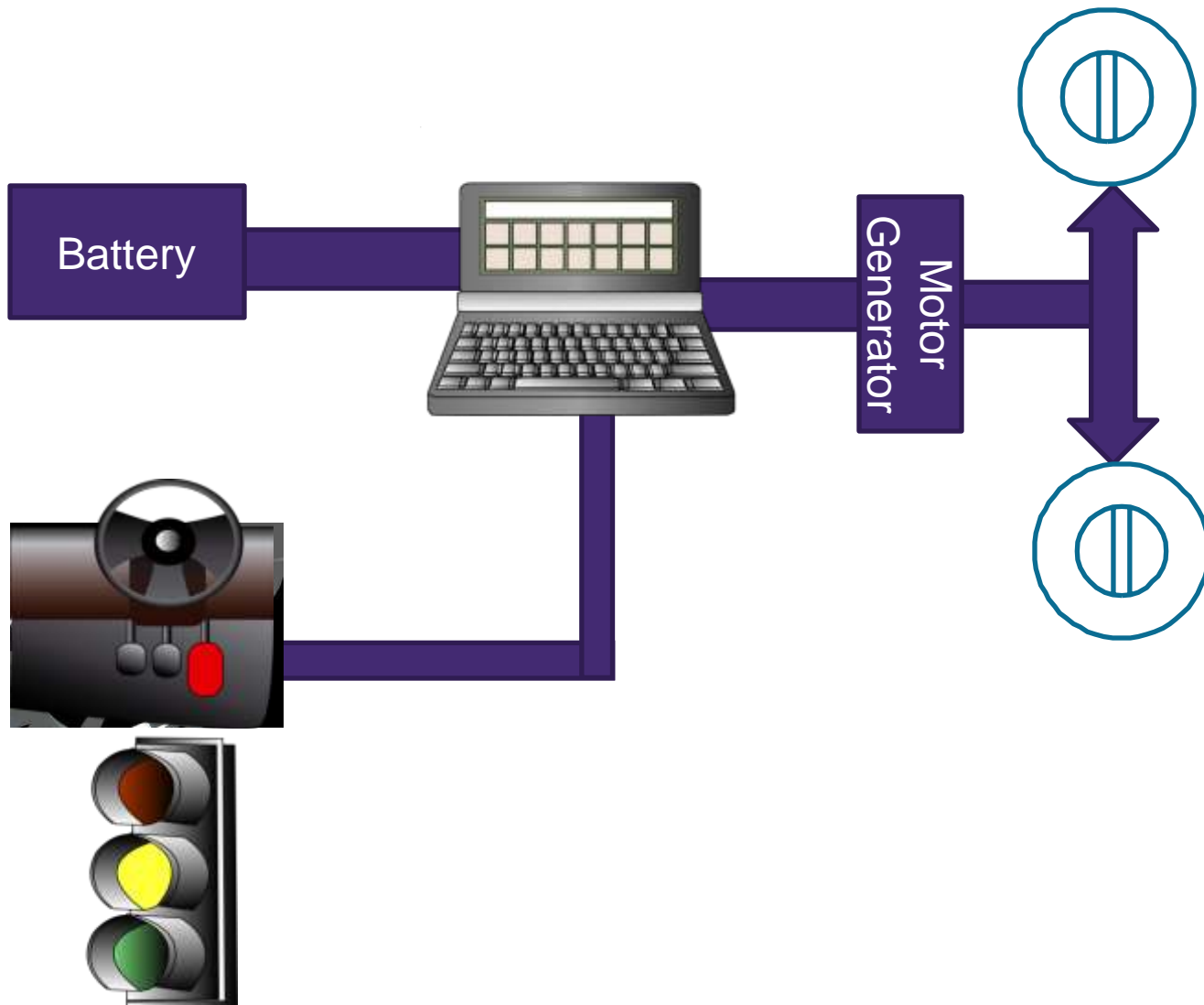
Recycle Energy - Hybrid Car



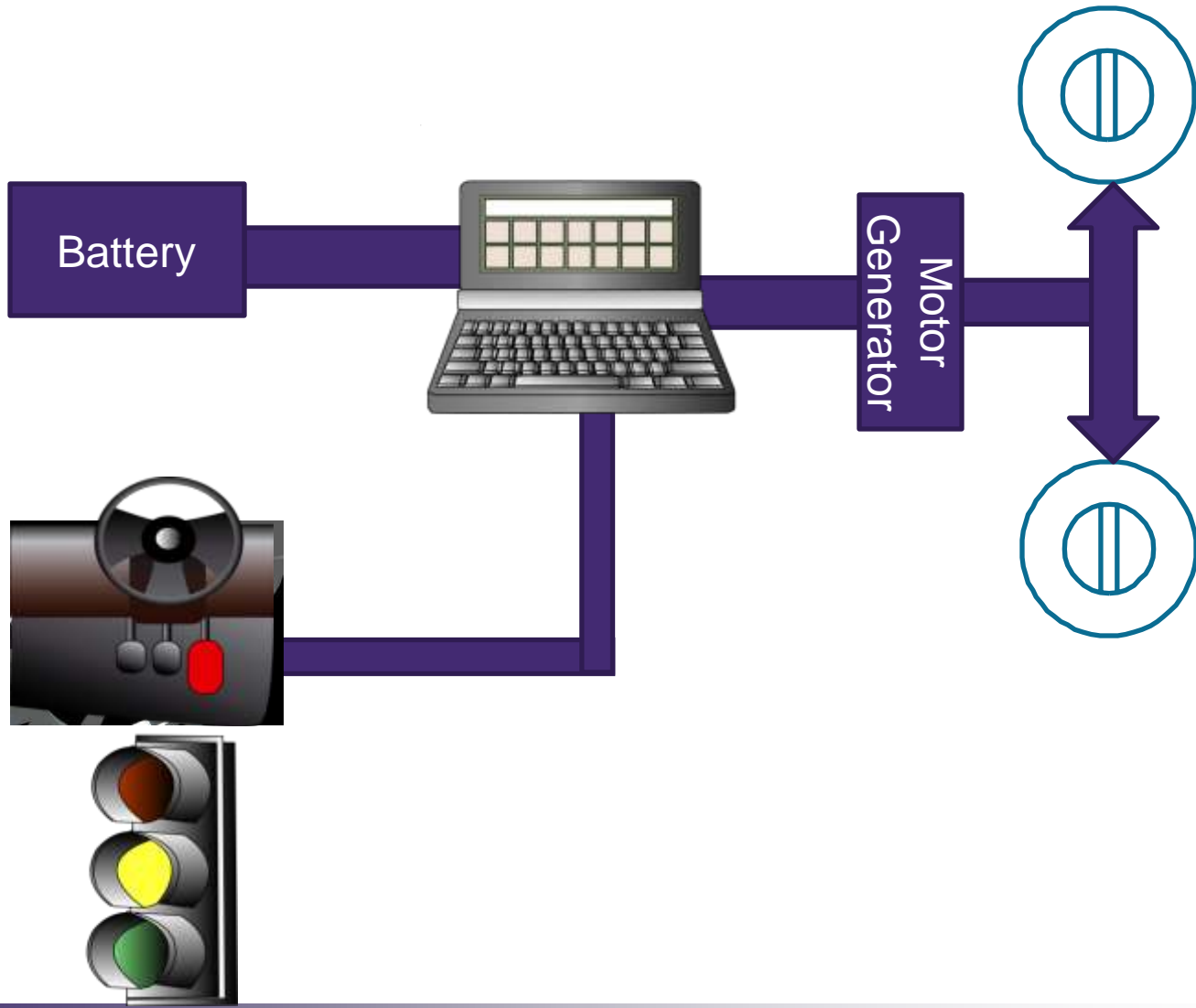
Recycle Energy - Hybrid Car



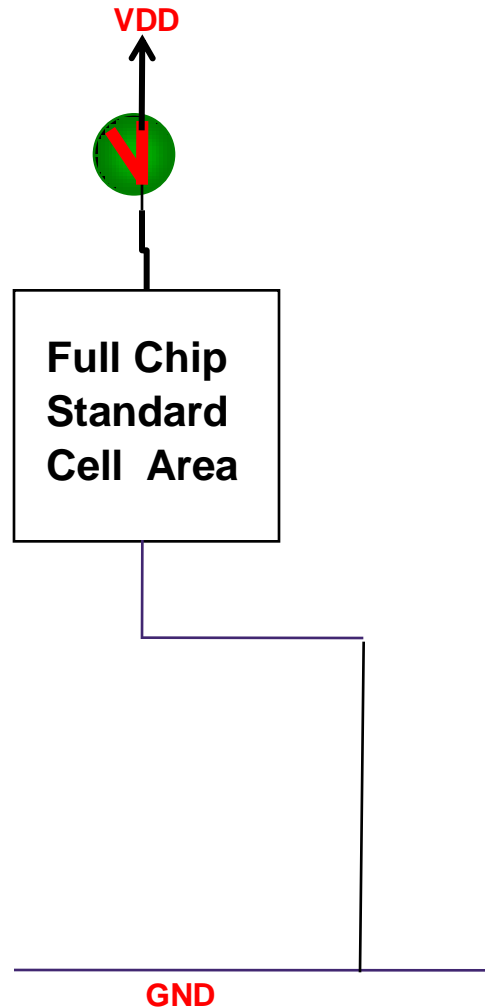
Recycle Energy - Hybrid Car



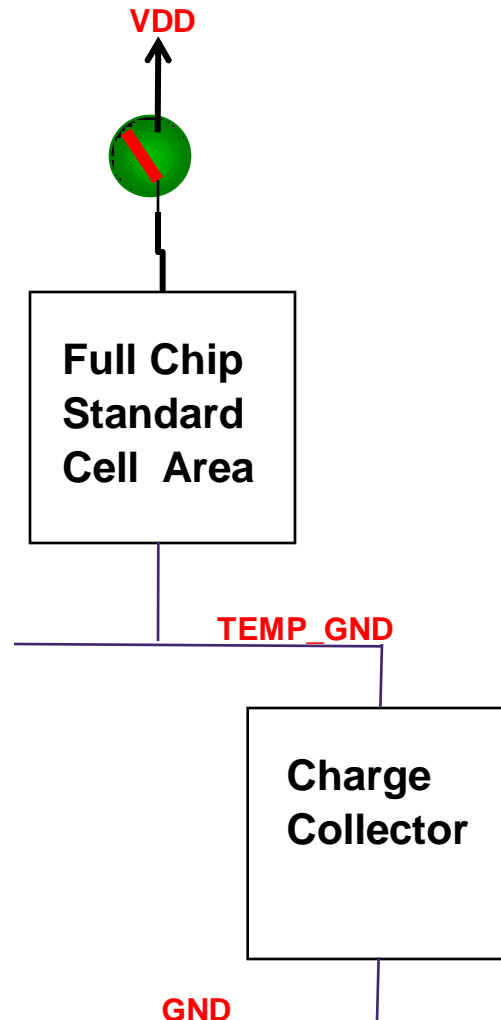
Recycle Energy - Hybrid Car



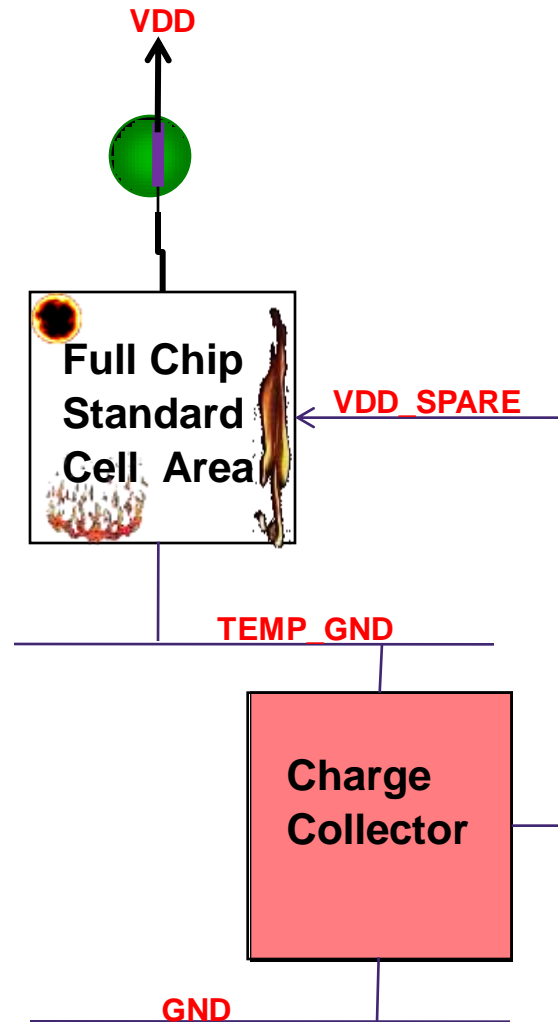
Recycle Leakage



Recycle Leakage

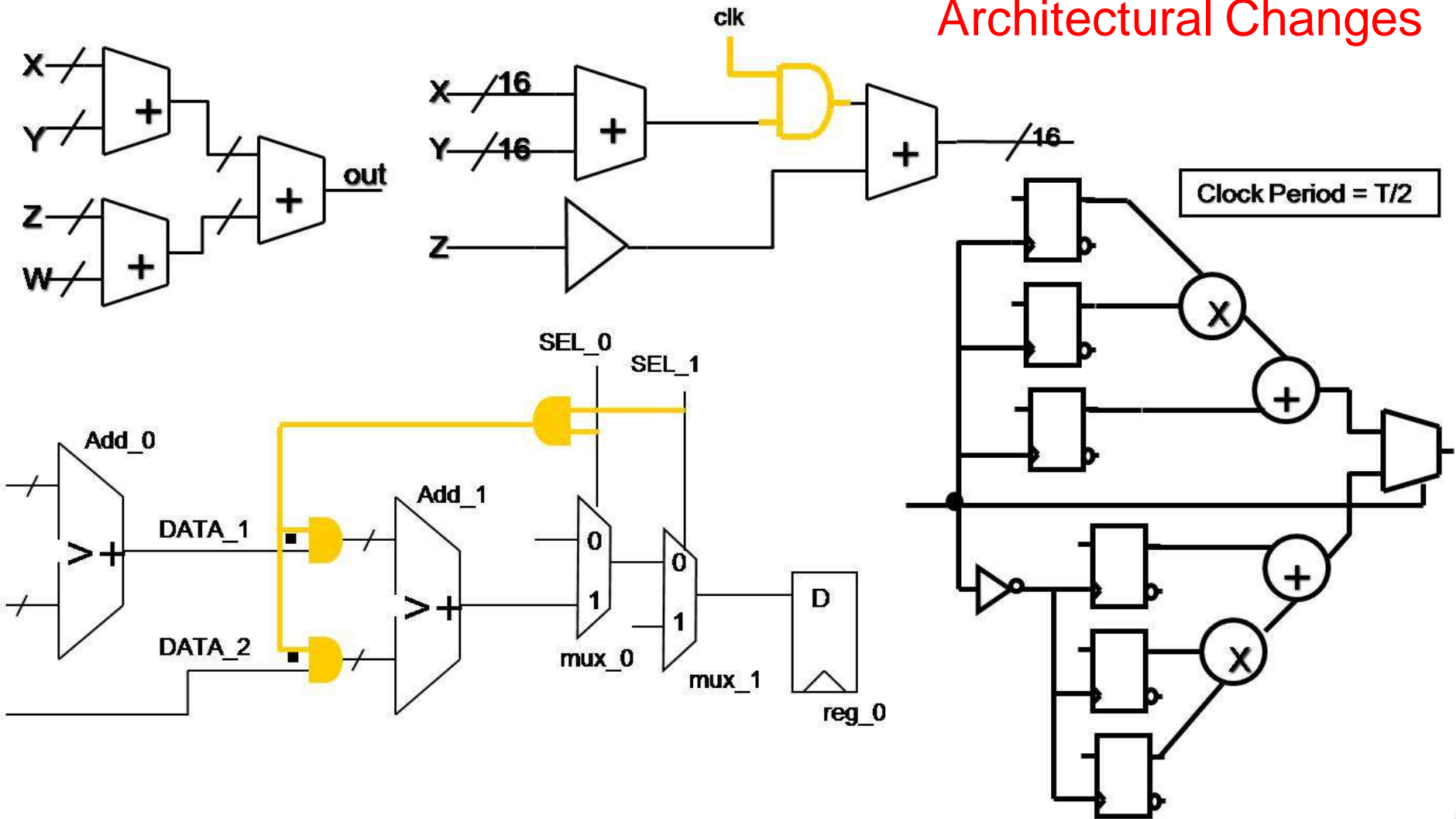


Recycle Leakage

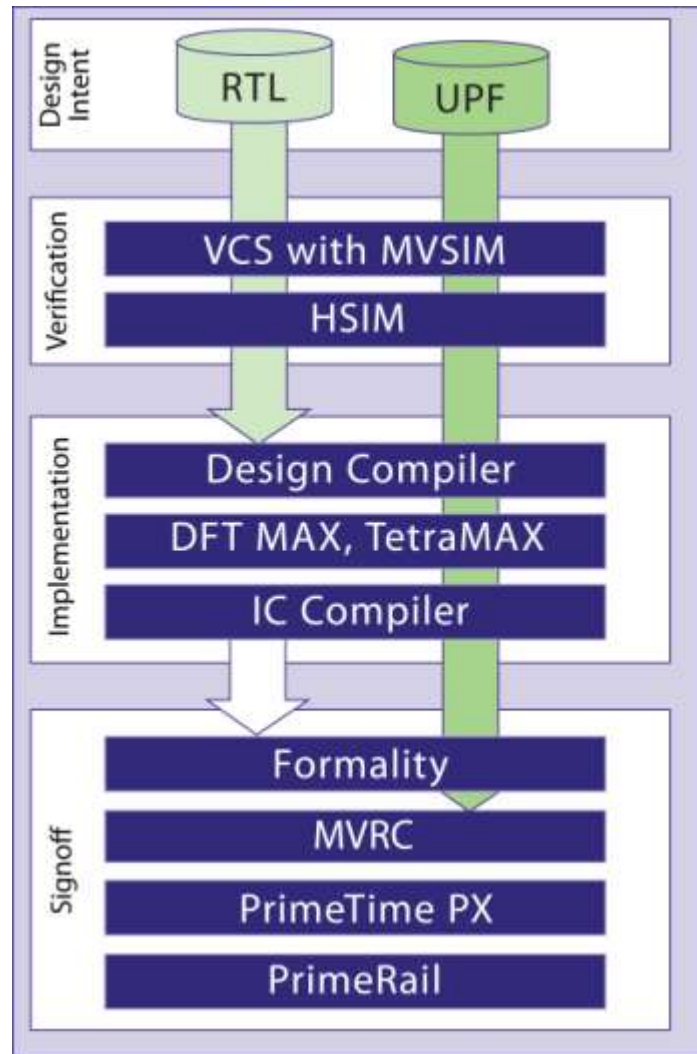


Where Best to Manage Power and How?

Architectural Changes



Synopsys Low Power Flow Summary



SYNOPSYS®

Predictable Success